Intel® Pentium® III Processor – Low Power/440BX AGPset

Design Guide

December 2002

Order Number: 273532-002

Contents

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Revision History

Date	Revision	Description
December 2002	002	Section 7.3.3, PLOCK# - In Pin Connection description, removed reference to PIIX4E in the second sentence. Section 7.3.5, Introductory bullet - Revised to state “To disable AGP, tie MAB9# high using a 10 K ohm pull-up to 3.3 V, connect GCLKO to GCLKIN through an 18 W resistor, and ground AGPREF. Section 7.3.6, DCLKWR - Revised Pin Connection description to state “22 Ω series termination at CKBFM. ‘T’ at the 22 Ω resistor with 15 pF cap to Vss.” Section 7.3.6, GCLKIN, Revised Pin Connection description to state “Connect to GCLKO through 18 Ω series resistor.” Section 7.4.5, IRQ [3:7, 9:11, and 14:15] - In Pin Connection description, added comma between 3:7 and 9:11. Section 7.4.5, PIRQ[A:D]# - In Pin Connection description, removed reference to 82443BX. Section 7.4.7, CLK48 - In Pin Connection description, added second sentence to state “When not using USB, the may be connected to GND.” Section 7.4.10, PCIREQ[A:D] - In Pin Connection description, added second sentence to state “Connect to 82443BX and PCI slots.” Section 7.4.10, RSMRST# - Added sentence to Pin Connection description to state “When not using power management (suspend modes), this may be connected to PIIX4E PWROK. Section 7.4.10, Vss (USB) - Removed reference as it is duplicated. Section 7.4.11, PWROK - Revised second sentence in Pin Connection description to state “When not using power management (suspend modes), also connect to PIIX4E RSMRST#.” Section 7.4.11, SPKR - Added sentence to Pin Connection description to state “NO CONNECT if not used.” Section 4.1.1 - Changed note for MAB[13] from Note #1 to Note #2.
August 2001	001	Initial release of this document.

1.0 Introduction

This document provides design guidelines for developing systems based on the Intel® Pentium® III processor – Low Power in a BGA2 package and the Intel® 440BX AGPset. System board and memory subsystem design guidelines are included. Special design recommendations and concerns are presented. Likely design errors have been listed here in a checklist format. These are recommendations only. It is recommended that you perform your own simulations to meet design-specific requirements.

Note: These guidelines also apply to the Intel® Celeron® processor – Low Power in a BGA2 package.

1.1 Key Terms

The Pentium® III processor – Low Power is specific to the applied computing market segment. A complete description of the processor is located in the *Intel® Pentium® III Processor – Low Power Datasheet* (order number 273500).

Intel 440BX AGPset refers to both the 82443BX Host Bridge/Controller and the 82371EB PCI ISA IDE Xcelerator.

82443BX refers to the Intel 82443BX Host Bridge/Controller.

PIIX4E refers to the Intel 82371EB PCI ISA IDE Xcelerator.

Design Features are items that allow the designer to fully use the capabilities of the Pentium III processor and the Intel 440BX AGPset.

Design Checklists are items which provide recommendations for designing an Pentium III processor – Low Power-based platform.

Design Considerations are items that should be considered but may not be applicable to your design.

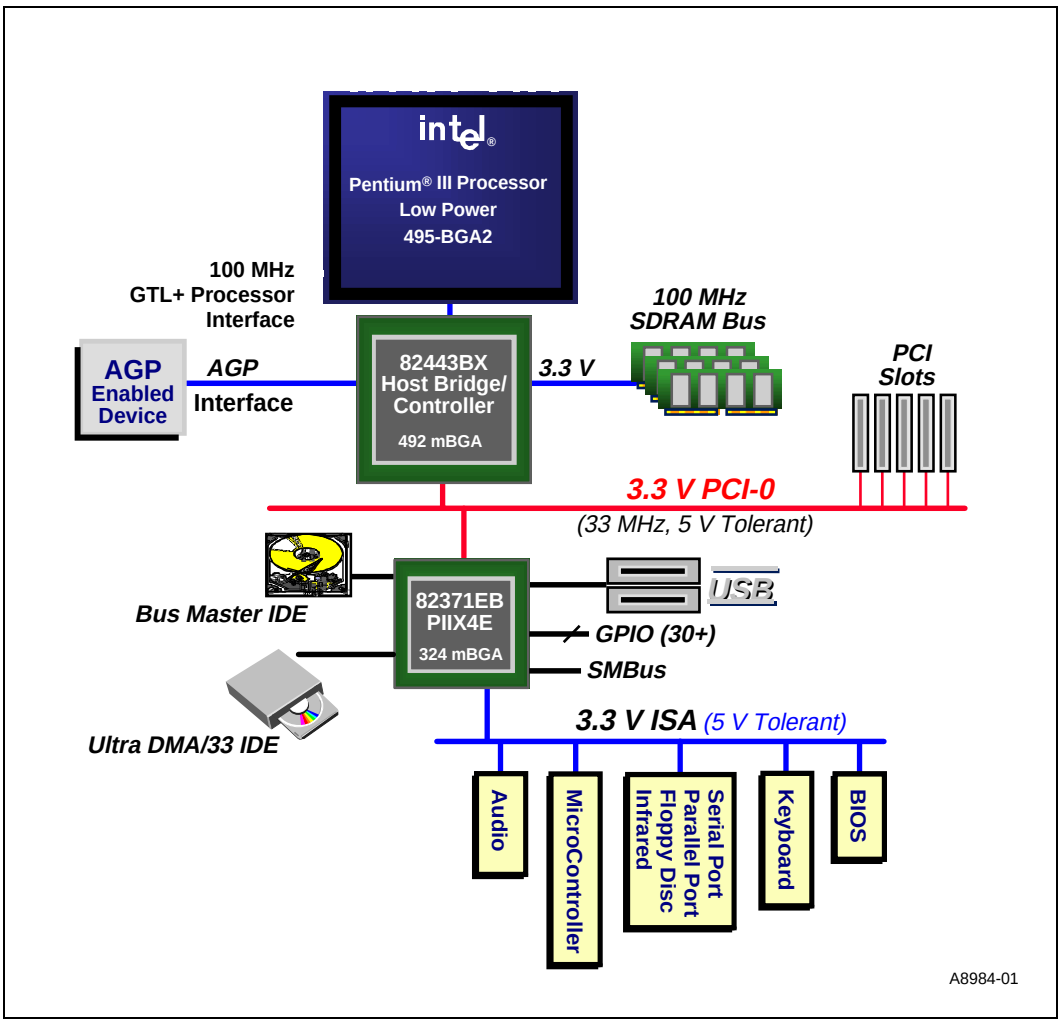
1.2 Overview

A Pentium III processor – Low Power/440BX AGPset system contains the features summarized below. Figure 1 is a block diagram of a typical Pentium III processor – Low Power/440BX AGPset system design.

- Full support for the Pentium® III processor – Low Power with system bus frequency of 100 MHz
- Intel 440BX AGPset
  - 82443BX Host Bridge/Controller (443BX)
  - 82371EB PCI ISA IDE Accelerator (PIIX4E)
- 100 MHz memory interface: A wide range of DRAM support including:
  - 64-bit memory data interface plus eight ECC bits and hardware scrubbing
  - 100 MHz SDRAM Support
  - 64-Mbit and 128-Mbit DRAM technologies

- Five PCI masters
  - — PCI Specification Rev 2.1 Compliant
- Accelerated Graphics Port (AGP) Slot:
  - — AGP Interface Specification Revision 1.0 compliant
  - — AGP - 66/133 MHz, 3.3 V device support
- Integrated IDE controller with Ultra DMA/33 support
  - — PIO Mode 4 transfers
  - — PCI IDE bus master support
- Integrated Universal Serial Bus (USB) controller with two USB ports
- Integrated System Power Management support

Figure 1. Intel® Pentium® III Processor – Low Power/440BX AGPset System Block Diagram



1.3 Related Documents

Table 1. Related Intel Documents

Document	Order Number
Intel® Pentium® III Processor – Low Power Datasheet	273500
Mobile Pentium® III Processor Specification Update	245306
Intel® 440BX AGPset: 82443BX Host Bridge/Controller Datasheet	290633
Intel® 440BX AGPset 82443BX Host Bridge/Controller Specification Update	290639
Intel® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) Datasheet	290562
Intel® 82371AB PIIX4E, Intel 82371EB PIIX4E and Intel 82371MB PIIX4M Specification Update	297738
Intel® Architecture Software Developer's Manual, Volume 1; Basic Architecture	243190
Intel® Architecture Software Developer's Manual, Volume 2; Instruction Set Reference	243191
Intel® Architecture Software Developer's Manual, Volume 3; System Programming Guide	243192
Intel® Architecture MMX™ Technology Developer's Guide	243006
Low Power Module SDRAM DIMM Routing Guidelines	273317
CK97 Clock Synthesizer Design Guidelines Application Note	243867
AP-485 *Intel Processor Identification and the CPUID Instruction Application Note*	241618
Pentium® III Processor Active Thermal Management Technology Application Note	273405
Intel® Pentium® III Processor - Low Power Thermal Design Guide	273285
PIIX4 Universal Serial Bus Design Guide and Checklist	NDA†

† NDA documents are only available through an Intel Field Sales Representative.

Table 2. Related Specifications

Document	URL/Contact
PCI Local Bus Specification, Revision 2.1	http://www.pcisig.com/specs.html
Universal Serial Bus Specification, Revision 1.1	http://www.usb.org/developers/docs.html
AGP Interface Specification, Revision 1.0	http://www.agpforum.org/index.htm
AGP Platform Design Guide, Revision 1.1A	http://www.agpforum.org/index.htm
System Management Bus Specification	http://www.sbs-forum.org/
66-MHz Unbuffered SDRAM 64-bit (Non-ECC/Parity) 144-pin SO-DIMM Specification, Revision 1.0	http://developer.intel.com/technology/memory/sodm1_0.htm
Universal Host Controller Interface (UHCI) Design Guide	http://developer.intel.com/design/USB/UHCI11D.htm

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2.0 Design Features

2.1 Intel® Pentium® III Processor – Low Power

The Intel® Pentium® III processor – Low Power is the first of the Pentium III processor family to be offered for the applied computing platform. It is offered in a 495 ball BGA2 package at 400 MHz, 500 MHz and 700 MHz with a processor system bus speed of 100 MHz. It consists of a Pentium III processor core with an integrated 256-Kbyte second-level cache and a 64-bit high-performance host bus. The second-level cache bus complements the host bus by providing critical data faster, improving performance, and reducing total system power consumption. The Pentium III processor – Low Power's 64-bit wide low power GTL+ host bus is compatible with the Intel® 440BX AGPset and provides a glueless, point-to-point interface for an I/O bridge and memory controller.

2.2 Intel® 440BX AGPset

The Intel® 440BX AGPset is based on the Pentium III processor architecture. It interfaces with the Pentium III processor's system bus at 100 MHz. Along with its Host-to-PCI bridge interface, the 82443BX Host Bridge/Controller has been optimized with a 100 MHz SDRAM memory controller and data path unit. The 82443BX also features the Accelerated Graphics Port (AGP) interface. The 82443BX component includes the following functions and capabilities:

- 64-bit Low Power GTL+ based system data bus interface
- 32-bit system address bus support
- 64-bit main memory interface with optimized support for SDRAM
- 32-bit PCI bus interface with integrated PCI arbiter
- AGP interface with up to 133 MHz data transfer capability
- Extensive data buffering between all interfaces for high throughput and concurrent operations

Figure 1 shows a block diagram of a typical platform based on the 440BX AGPset. The 82443BX system bus interface supports a Pentium III processor at a bus frequency of 100 MHz. The physical interface design is based on the Low Power GTL+ specification and is compatible with the Intel 440BX AGPset. The 440BX provides an optimized 72-bit DRAM interface (64-bit Data plus ECC). This interface supports 3.3 V DRAM technologies.

The 82443BX is designed to support the PIIX4E PCI-to-ISA bridge. The PIIX4E is a highly-integrated multifunctional component that supports the following functions and capabilities:

- PCI Revision 2.1 compliant PCI-to-ISA bridge with support for 33 MHz PCI operations
- ACPI Power Management support
- Enhanced DMA controller, interrupt controller and timer functions
- Integrated IDE controller with Ultra DMA/33 support
- USB host interface with support for two USB ports
- System Management Bus (SMB) with support for DIMM Serial Presence Detect

2.2.1 System Bus Interface

The 82443BX supports a maximum of 4 Gbytes of memory address space from the processor perspective. The largest address size is 32 bits. The 82443BX provides bus control signals and address paths for transfers between the processor bus, PCI bus, Accelerated Graphics Port and main memory. The 82443BX supports a 4-deep-in-order queue, which provides support for pipelining of up to four outstanding transaction requests on the system bus. The Pentium III processor supports a second-level cache. All cache-control logic is provided on the processor.

For system bus-to-PCI transfers, the addresses are either translated or directly forwarded on the PCI bus, depending on the PCI address space being accessed. When the access is to a PCI configuration space, the processor I/O cycle is mapped to a PCI configuration space cycle. When the access is to a PCI I/O or memory space, the processor address is passed without modification to the PCI bus. Certain memory address ranges are dedicated for a graphics memory address space. When this space or a portion of it is mapped to main DRAM, the address is translated by the AGP address remapping mechanism and the request is forwarded to the DRAM subsystem. A portion of the graphics aperture may be mapped on the AGP, and the corresponding system bus cycles accessing that range are forwarded to the AGP without any translation. The AGP address map defines other system bus cycles that are forwarded to the AGP.

2.2.2 DRAM Interface

The 82443BX integrates a main memory controller that supports a 64-bit DRAM interface which operates at 100 MHz. The integrated DRAM controller features include:

- 3.3 V interface
- Support for up to three double-sided SODIMMs
  - 384 Mbytes using 128-Mbit technology
  - 192 Mbytes using 64-Mbit technology
  - 48 Mbytes using 16-Mbit technology
- Support for ECC with hardware scrubbing

2.2.3 Accelerated Graphics Port Interface

The 82443BX supports an AGP interface. The AGP interface has a maximum theoretical transfer rate of ~532 Mbytes/s.

2.2.4 PCI Interface

The 82443BX PCI interface operates at 3.3 V (5 V tolerant), 33 MHz, is Revision 2.1 compliant, and supports up to five external PCI bus masters in addition to the PIIX4E I/O bridge.

2.2.5 System Clocking

Used with the Pentium® III processor, the 82443BX operates the system bus interface at 100 MHz, the PCI bus at 33 MHz and the AGP at a transfer rate of 66/133 MHz. The 82443BX clocking scheme uses an external clock synthesizer that produces reference clocks for the system bus and PCI interfaces. The 82443BX generates the AGP and DRAM clock signals. Please refer to the *CK97 Clock Synthesizer/Design Guidelines Application Note* (order number 243867).

2.3 PCI ISA IDE Xcelerator (PIIX4E)

The PCI ISA IDE Xcelerator (PIIX4E) is a multi-function PCI device that implements a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus host/hub function, and an Enhanced Power Management function. Because it is a PCI-to-ISA bridge, the PIIX4E integrates many common I/O functions found in ISA-based PC systems; a seven channel DMA Controller, two 82C59 Interrupt Controllers, an 8254 Timer/Counter, and a Real Time Clock. In addition to DMA Compatible transfers, each DMA channel also supports Type F transfers.

The PIIX4E contains full support for PC/PCI and Distributed DMA protocols that implement PCI-based DMA. The Interrupt Controller has edge or level sensitive programmable inputs. Chip select decoding is provided for a BIOS, Real Time Clock, Keyboard Controller, second external microcontroller, and two Programmable Chip Selects. The PIIX4E provides full Plug-and-Play compatibility. The PIIX4E may be configured as a subtractive decode bridge or as a positive decode bridge.

The PIIX4E supports two IDE connectors. This provides an interface for IDE/EIDE hard disks and CD-ROMs. Up to four IDE devices may be supported in Bus Master mode. The PIIX4E contains support for Ultra DMA/33 compatible synchronous DMA devices.

The PIIX4E contains a Universal Serial Bus (USB) host controller that is Universal Host Controller Interface (UHCI) compatible. The host controller's root hub has two programmable USB ports.

The PIIX4E supports Enhanced Power Management, including full clock control, device management for up to 14 devices, and suspend and resume logic with Power On Suspend, Suspend to RAM, or Suspend to Disk. The PIIX4E fully supports operating-system-directed power management according to the Advanced Configuration and Power Interface (ACPI) specification. The PIIX4E integrates both a System Management bus (SMBus) host and slave interface for serial communication with other devices.

For more information on the PIIX4E, please refer to the *Intel® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) Datasheet* (order number 290562) and the *Intel® 82371AB PIIX4, Intel® 82371EB PIIX4E and Intel® 82371MB PIIX4M Specification Update* (order number 297738).

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3.0 System Bus Guidelines

This section provides the guidelines required for the Pentium® III processor – Low Power and 82443BX bus portion of the PCB layout. The guidelines and methodologies do not provide absolute rules. They include recommendations on Processor System Bus (PSB) routing topologies and system board impedance. Even when the guidelines are followed, it is strongly recommended that you run analog simulations using the available I/O buffer models together with layout information extracted from your specific design.

3.1 Definitions

Frequently used abbreviations are defined below:

Aggressor - A network that transmits a coupled signal to another network is called the aggressor network.

Bus Agent - A component or group of components that, when combined, represent a single load on the GTL+ bus.

Corner - Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in the manufacturing process, the operating temperature, and the operating voltage. The results in performance of an electronic component that may change as a result of this include but are not limited to: clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the ‘slow’ corner means having a component operating at its slowest, weakest performance. Similar discussion of the ‘fast’ corner means having a component operating at its fastest, strongest performance. Operation or simulation of a component at its slow corner and fast corner is expected to bind the extremes between slowest, weakest performance and fastest, strongest performance. The component packages, printed circuit boards and electrical connectors also have corner characteristics that effect Pentium III processor-Low Power based system designs.

Crosstalk - The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.

Backward Crosstalk - Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal.

Even Mode Crosstalk - Coupling from one or more aggressors when all the aggressors switch in the same direction that the victim is switching.

Forward Crosstalk - Coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal.

Odd Mode Crosstalk - Coupling from one or more aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Flight Time - The additional delay between the driver and receiver introduced by the printed circuit board interconnects and the component loading effects as compared to the data sheet specification load. Although the name implies that this is the time required for a signal to travel from one end of the interconnect to the other, a better definition of this term is simply that it is the total delay the layout (interconnects plus loads) adds to the component timings. (This is similar to the usage of the term ‘derating’, but that term fails to acknowledge that transmission line effects are being included in the analysis.) Flight time is therefore defined as the difference between when a signal at the input pin of a receiving agent crosses V_{REF} and the time that the output pin of the driving agent crosses the V_{REF} were it driving the test load used

to specify that driver's AC timings. V_{REF} for the Pentium III processor- Low Power is 2/3 of V_{CCT}. ($V_{CCT} = V_{TT}$)

Flight time is defined as:

$$T_{FLIGHT} = T_{RECEIVER} - T_{REF}$$

where T_{REF} is the reference delay discussed above, and $T_{RECEIVER}$ is the time at which the waveform has a valid V_{REF} crossing.

Figure 2 and Figure 3 show the definition of flight time. Notice that determining flight time requires a minimum of two simulations, one in which the driver is driving the test load, and one in which it is driving the actual system load. Also note that this method introduces the concept of negative flight time, as seen in Figure 3.

Figure 2. Definition of the Flight Time Criteria - Falling Edge

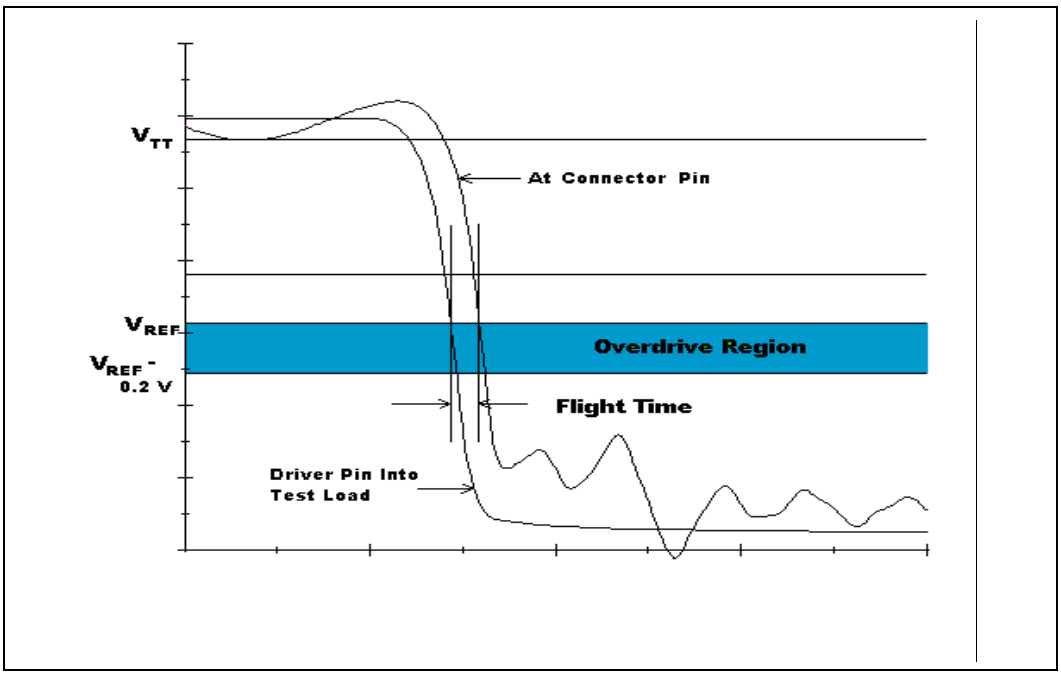
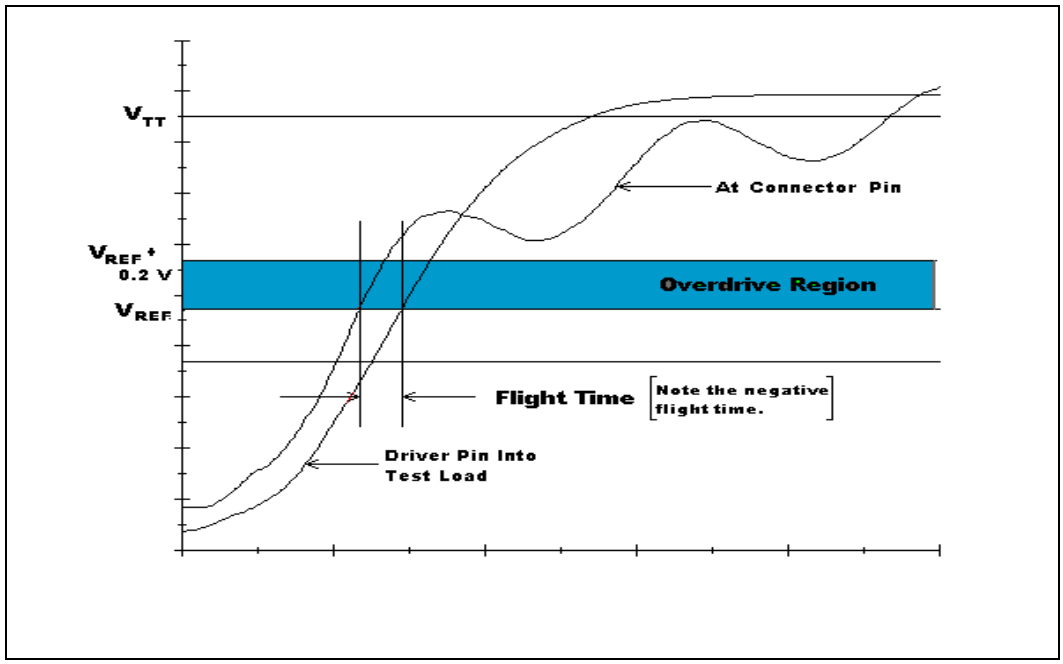


Figure 3. Definition of the Flight Time Criteria - Rising Edge



Maximum and Minimum Flight Time - Flight time variations may be caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of multiple signals switching and additional packaging affects. Table 4 includes recommended adjustment factors.

Maximum Flight Time – This is the largest flight time a network will experience under all variations of conditions.

Minimum Flight Time - This is the smallest flight time a network will experience under all variations of conditions.

FSB - Front Side Bus, a reference to the GTL+ bus on the front of the Pentium III processor – Low Power, as opposed to the cache or backside bus. This nomenclature is not used in this document. Please see PSB.

GTL+ - The bus technology used by the Pentium III processor – Low Power. This is an incident wave switching, open drain bus with internal pullups at the processor that provide both the high logic level and termination at each processor end of the bus. It is an enhancement to the GTL+(Gunning Transceiver Logic) technology. Refer to the *Pentium® II Processor Developer's Manual* for more information.

Low Power GTL+ - A modification of the GTL+ bus technology for use in low power applied computing applications.

Network - The trace of a Printed Circuit Board (PCB) that completes an electrical connection be tween two or more components.

Network Length - The distance between extreme bus agents on the network and does not include the distance connecting the end bus agents to the termination resistors.

Northbridge - The system logic component that interfaces directly to the processor's PSB.

OEM - Original Equipment Manufacturer.

Overdrive Region - The voltage range, at a receiver, from V_{REF} to V_{REF} + 200 mV for a low to high going signal and V_{REF} to V_{REF} - 200 mV for a high to low going signal.

Overshoot - A voltage amplitude that exceeds the maximum voltage, V_{IH}, level as specified in the component specification.

PSB - Processor System Bus, a reference to the Low Power GTL+ bus on the Pentium III processor – Low Power.

Ringback - The re-crossing of a high or low input logic threshold after it has initially crossed that logic threshold.

Settling Limit - The maximum allowed peak to peak oscillation after a signal has transitioned to the correct logic level as specified in the component specification.

Setup Window - The time between the beginning of Setup to Clock (T_{SU_MIN}) and the clock input.

Undershoot - A voltage amplitude that negatively exceeds the minimum low voltage, V_{IL} level as specified in the component specification.

Victim - A network that receives a coupled crosstalk signal from another network is called the victim network.

3.2 Recommended Low Power GTL+ Design Guideline

The following step-by-step guideline was developed for systems based on one Pentium III processor – Low Power and one 82443BX load. The methodology recommended in this section is based on experience developed at Intel while developing many different Pentium III processor-based systems for validation and feasibility studies. This methodology relies on spreadsheet type calculations for initial timing analysis and performing signal integrity/noise analysis. The analog simulations should be validated after actual systems become available.

3.2.1 Components

The GTL+ PSB is restricted to two agents: the Pentium III processor – Low Power and the 82443BX.

3.2.2 Initial Timing Analysis

An initial timing analysis of the system is required. To complete the timing analysis, values for the clock skew and clock jitter are needed with the component specifications. These values should be sufficient for determining the bounds for system flight times. Equation 1 and Equation 2 are the basis for the timing analysis.

Equation 1. Maximum Frequency

$$\text{Clock Period} \geq T_{FLIGHT\_MAX} + T_{CO\_MAX} + T_{SU\_MIN} + CLK_{SKEW} + CLK_{JITTER} + T_{ADJ\_SU}$$

Equation 2. Hold Time

$$T_{CO\_MIN} + T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} + T_{ADJ\_Hold}$$

Symbols used in Equation 1 and Equation 2:

T_{CO_MAX} - the maximum clock to output specification.[1]

T_{CO_MIN} - the minimum clock to output specification.[1]

T_{SU_MIN} - the minimum required time specified to setup before the clock.[1]

T_{HOLD} - the minimum specified input hold time.

T_{ADJ} - an empirical timing adjustment factor that accounts for timing 'push out' or 'pull in' seen when multiple bits change state at the same time. The factors that contribute to the adjustment factor include crosstalk on the PCB, substrate, and packages, simultaneous switching noise, and edge rate degradation caused by inductance in the ground return path.[2] This number is also sometimes called Tsso. The SSO stands for Simultaneous Switching Output. This adjustment is for board SSO, not chip SSO, as chip SSO numbers are included in the Tco specification of the device.

CLK_{JITTER} - the maximum clock edge to edge variation.

CLK_{SKEW} - the maximum variation between components receiving the same clock edge.

T_{FLT_MAX} - the maximum flight time as defined in Section 3.1.

T_{FLT_MIN} - the minimum flight time as defined in Section 3.1.

NOTES:
1. The Clock to Output (T_{CO}) and Setup to Clock (T_{SU}) timings are both measured from the signals last crossing of V_{REF}, with the requirement that the signal does not violate the ringback or edge rate limits. See the *Pentium® II Processor Developer's Manual* for more details.
2. T_{ADJ} should be calculated for each individual system. A value of 0.5 ns is used throughout this document and may be used as a generic T_{ADJ} value during flight time calculations if an actual crosstalk flight time delay may not be calculated.

Solving these equations for flight time results in the following equations:

Equation 3. Maximum Flight Time

$$T_{FLIGHT\_MAX} = \text{Clock Period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - T_{ADJ\_SU}$$

Equation 4. Minimum Flight Time

$$T_{FLIGHT\_MIN} = T_{HOLD} + CLK_{SKEW} + T_{ADJ\_Hold} - T_{CO\_MIN}$$

There are two cases to consider. Note that while the same trace connects two components (e.g., A and B), the minimum and maximum flight time requirements for A driving B as well as B driving A must be met. The cases discussed in this document are:

Pentium III processor – Low Power driving the 82443BX

82443BX driving the Pentium III processor – Low Power

GTL+ trace lengths required to meet these timings may be calculated using the maximum and minimum flight time calculations and the effective board propagation constant (S_{EFF}). S_{EFF} is a function of:

Dielectric constant (ε_r) of the PCB material

The type of trace connecting the components (stripline or microstrip)

The length of the trace and the load of the components on the trace. (Note that the board propagation constant multiplied by the trace length is a **component** of the flight time but **not necessarily equal** to the flight time.)

3.2.3 Determine General Layout, Routing and Topology

Once the processor bus components have been selected and the timing budget calculated, then determine their approximate location on the printed circuit board. Estimate the printed circuit board parameters from the placement and other information including the following general layout and routing given below:

Figure 4. Pentium® III Processor – Low Power General GTL+ Interconnect and Topology Guidelines

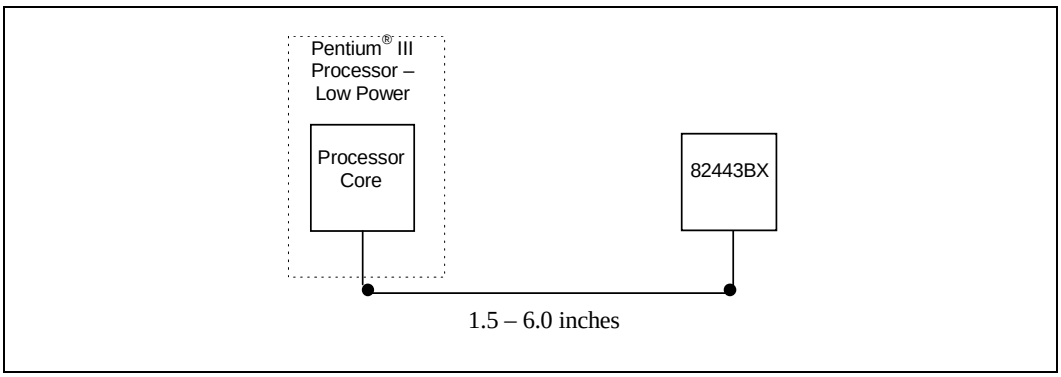
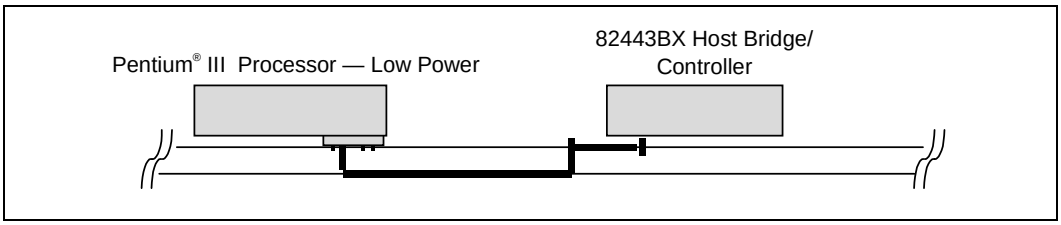


Figure 5. Processor Routing Example



General recommendations for Low Power GTL+ bus topology, layout, and routing are given in the following list. Also refer to Figure 4 and Figure 5.

- The net **must not** exceed 6.0 inches and **must exceed** 1.5 inches.
- Closely control the characteristic line impedance, Z_0 = 55Ω +/- 10%.
- PSB Traces should all be internal traces except for the breakout from the processor or chipset, which should not exceed 75 mils.
- Successive dual-stripline trace layers should be routed orthogonally.
- Trace width and spacing should be at least 4/6. (Trace width and spacing of 4/8 is even better. Do not route 5/5 except as necessary within the area of the processor or chipset.)
- Triple and Quad-stripline stackups are discouraged. When these types of stackups are used, Intel recommends a rigorous post-layout validation of the design including crosstalk analysis.

- Route the same type of Low Power GTL+ I/O signals in isolated signal groups. That is, route the data signals in one group, the address signals in another group. Keep at least 12 mils between each group of signals.
- Minimize use of vias.
- Maximum parallel- trace routing length is 3.5 inches (at 4/6).
- Always be sure to validate signal quality after making any changes in agent locations or changes to inter-agent spacing.
- This document addresses Low Power GTL+ layout. Other chassis requirements including cooling, mechanical stability, and memory location may constrain the system topology and component placement location; therefore constraining the board routing. These issues are not directly addressed in this document.

3.2.4 Estimate Component to Component Spacing for Low Power GTL+ Signals

After determining the general layout, do a more specific preliminary component placement. Estimate the number of layers that will be required. Then determine the expected interconnect distances between the components on the Low Power GTL+ bus. Using the estimated interconnect distances, verify that the placement may support the system timing requirements.

Figure 6. Pentium® III Processor- Low Power Component Placement Example

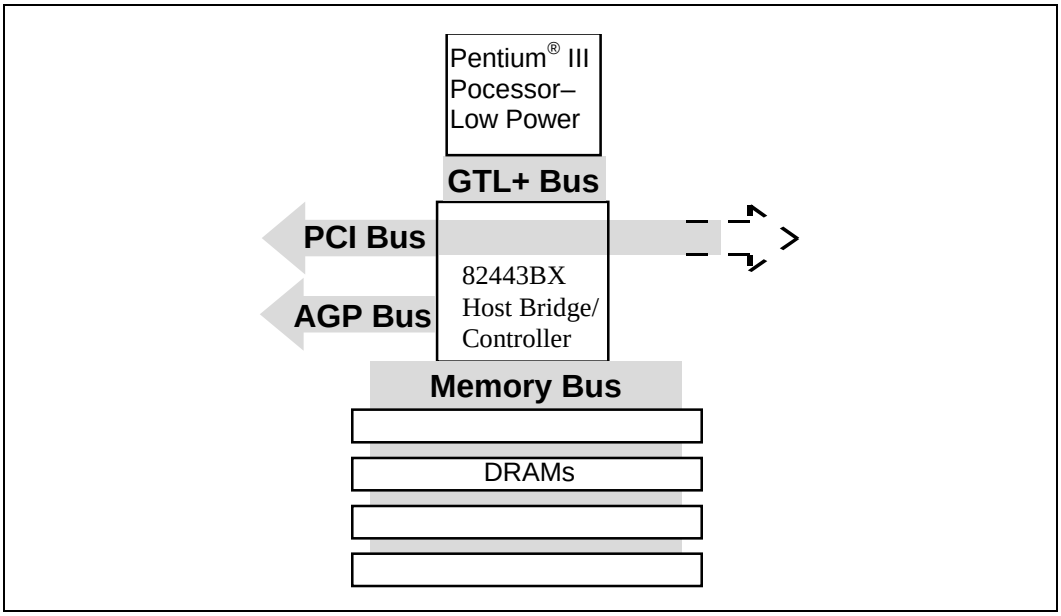


Figure 6 shows one example of a Pentium III processor – Low Power based system component placement.

The maximum network length between the bus agents is determined by the bus frequency and the maximum flight time propagation delay on the PCB. The minimum network length is independent of the required bus frequency. The equations DO NOT allow for any change in the propagation of the signal due to ringback, crosstalk on the network/package, or for any difference in buffer

performance caused by driving actual loaded transmission lines instead of test loads that are used in the component specification. Intel suggests running analog simulations to ensure that each design has adequate noise and timing margin.

After the board layout is complete, extract real trace lengths and run analog simulations to verify the actual layout meets the timing and noise requirements.

3.3 Simulation

3.3.1 Overview

Intel strongly suggests running analog simulations for Pentium III processor – Low Power designs. Intel provides the Pentium III processor – Low Power I/O Buffer Models and the 82443BX I/O Buffer Models in IBIS 2.1 format. These models are available from your local Intel Field Sales Representative. Accurate simulations require that the actual range of parameters be used in the simulations.

Positioning drivers with faster edges closer to the middle of the network results in more noise than positioning them towards the ends. Intel has seen that the worst-case noise margin may be generated by drivers located in all positions (given appropriate variations in the other network parameters). Therefore, stimulating the networks from all driver locations and analyzing each receiver for each possible driver is recommended. Simulate using both values of R_{TT} in the Pentium III processor – Low Power IBIS model.

Faster edge rates cause increased ringback, which reduces the noise margin on the rising edge (Low to High); therefore, only the fast corner (voltage, temperature, and process) I/O buffer model needs to be simulated for the Low to High transitions to evaluate signal quality. Analysis has also shown that both fast and slow models must be run to verify signal quality on the falling edge (High to Low). The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be a minimum causing the V_{OL} to shift up, which may cause the noise from the slower edge to exceed the available budget. The slow corner I/O buffer model is used to check the maximum flight time.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. Likewise, the package model must also be placed between a net and the input of a receiver model. This is generally done by editing your simulator's net description or topology file.

3.3.2 Extract Interconnect Information

Extract the actual interconnect information for the board from the CAD layout tools.

3.3.3 Run Simulations

For timing and signal integrity analysis at the Pentium III processor – Low Power connector pins, simulations need to be performed using the fast/slow buffer models, board impedance and the dielectric extreme values, and V_{TT} and R_{TT} extremes. As shown in Equation 3 and Equation 4, both the minimum and maximum lengths need to be simulated.

For timing simulations use a V_{REF} voltage of 2/3 V_{CCT} ± 2% for both the Pentium III processor – Low Power and 82443BX. R_{TT} for the Pentium III processor – Low Power is an idealized 50-65Ω internal resistor pulled up to V_{CCT}. Flight times measured from the Pentium III processor- Low Power connector pins to other system components use the standard method of subtracting the reference delay with this load from the delay to the destination component at 2/3 V_{CCT}.

3.4 Summary of System Design Guidelines

A quick summary of the board design guidelines presented in Section 3.0 is shown in Table 3.

Table 3. Summary of Board Design Guidelines

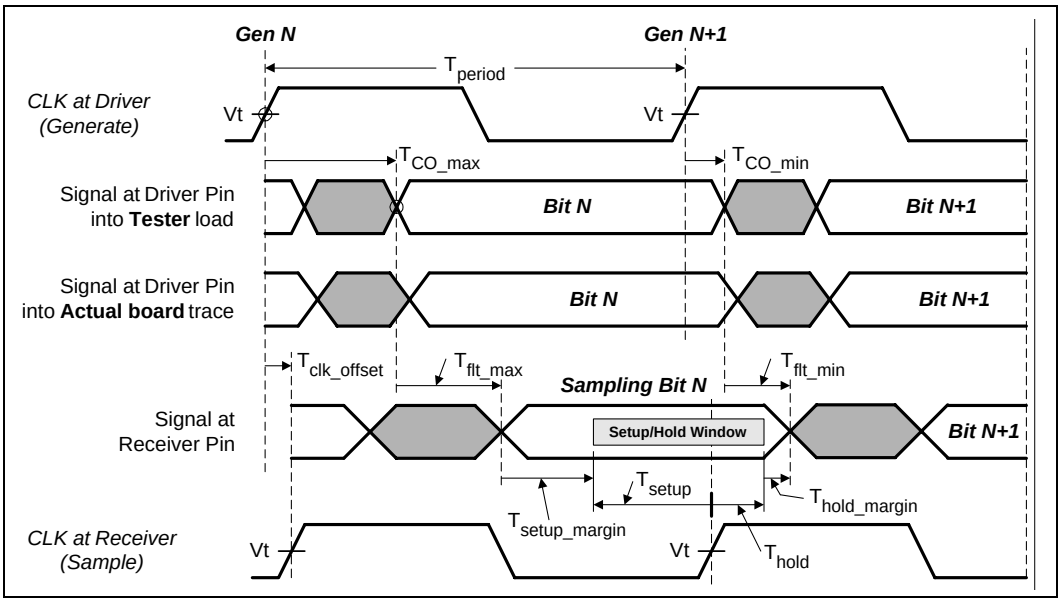
Parameter	Value	Units
Pentium III processor- Low Power to 82443BX Trace length	1.5 – 6.0	inches
Trace line impedance	55 +/-10%	ohms
Trace line width	4	mils
Trace line spacing	>= 6	mils
Breakout from Package	75	mils
FR4 dielectric constant	3.9-4.5	n/a
Maximum Parallel Routing	3.5	inches
Traces Internally Routed (Stripline or Dual-Stripline)		

- The Pentium III processor – Low Power has on-die R_{TT}. The RESET# signal needs an off-die 56.2Ω ± 1% resistor pulled-up to V_{CCT}.
- The 82443BX GTL+ buffers are programmed for Low Power GTL+ setting (vs. desktop GTL+ choice) by strapping MAB6# high. See the Design Checklist in Section 7.0 for 82443BX strapping options.

3.5 Timing Diagram for Processor Side Bus

Figure 7 illustrates the timing concepts for the processor side bus.

Figure 7. Processor Side Bus Timing Concepts



4.0 Memory Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order in which signals are routed first and last will vary from designer to designer. Some designers prefer routing the clock signals first, while others prefer routing the high-speed bus signals first. Either order may be used, as long as the guidelines listed here are followed. When the guidelines listed here are not followed, it is very important to simulate the design. Even when the guidelines are followed, it is recommended that you simulate these signals for proper signal integrity, flight time and cross talk.

4.1 100 MHz SDRAM Interface Overview

The 82443BX integrates a main memory DRAM controller that supports a 64-bit or 72-bit (64 bit memory data plus 8 bit ECC) DRAM array for 100 MHz embedded environments. A Pentium® III processor – Low Power/440BX system supports Synchronous DRAM (SDRAM); it does not support EDO memory. The 82443BX DRAM interface runs at 100 MHz. The DRAM controller interface is fully configured through a set of control registers. Complete descriptions of these registers are given in the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller Datasheet* (order number 290633).

The 443BX supports industry standard 64-bit wide 144-pin SODIMM modules with SDRAM devices. Both symmetric and asymmetric addressing is supported. For write operations of less than a Qword in size, the 443BX will either perform a byte-wide write cycle (non-ECC protected configuration) or a read-modify-write cycle by merging the write data on a byte basis with the previously read data (ECC or error correction configurations). The 82443BX requires SDRAM with CAS latency of 2 (CL2), and supports 1-and 2-row SODIMMs. The 82443BX provides refresh functionality with programmable rates (normal DRAM rate is 1 refresh/15.6 µs).
The 82443BX may be configured through the paging policy register to keep multiple pages open within the memory array. Pages may be kept open in all rows of memory. When using two bank SDRAM devices in a particular row, up to two pages may be kept open within that row.

The DRAM interface of the 82443BX is configured by the DRAM control registers, DRAM timing register, SDRAM control register, bits in the NBXCFG register and the eight DRAM row boundary (DRB) registers. The DRAM configuration registers control the DRAM interface to select EDO or SDRAM, RAS timing, and CAS rates. The eight DRB registers define the size of each row in the memory array, enabling the 82443BX to assert the proper CSA[7:0]#, CSB[7:0]# pair for accesses to the array.

4.1.1 SDRAM Signal Description

The following sections explain which signals are used in applied computing platforms, and how they should be connected. Note that MAB[13,10] are not inverted because these address bits are used to define various SDRAM commands.

Table 4 identifies the SDRAM signals and the corresponding description.

Table 4. SDRAM Signal Descriptions

Name	Type	Voltage	Description
MECC[7:0][1]	I/O CMOS	V_3	**Memory ECC Data:** These signals carry Memory ECC data during access to DRAM.
CSA[5:0]#	O CMOS	V_3	**Chip Select (SDRAM):** These pins activate SDRAM. SDRAM accepts any command when its CS# pin is active low.
DQMA[7:0]	O CMOS	V_3	**Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.
MAB[9:0]# MAB[10][2] MAB[12:11]# MAB[13][2]	O CMOS	V_3	**Memory Address (SDRAM):** This is the row and column address for DRAM. The 443BX Host Bridge system controller has two identical sets of address lines (MAA and MAB#). The recommendations in this design guide are based on the use of only one set of address lines. For additional addressing features, please refer to the *Intel® 440BX AGPset: 82443BX Host Bridge/ Controller Datasheet* (order number 290633).
MWEA#	O CMOS	V_3	**Memory Write Enable (SDRAM):** MWEA# should be used as the write enable for the memory data bus.
SRASA#	O CMOS	V_3	**SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge.
SCASA#	O CMOS	V_3	**SDRAM Column Address Strobe (SDRAM):** When active low, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access.
CKE[5:0]	O CMOS	V_3	**SDRAM Clock Enable (SDRAM):** The SDRAM clock enable pin. When these signals are deasserted, SDRAM enters power-down mode. Each row is individually controlled by its own clock enable.
MD[63:0]	I/O CMOS	V_3	**Memory Data:** These signals are connected to the DRAM data bus.

NOTES:
1. MECC[7:0] signals on the 82443BX may be left unconnected if the design does not support ECC. For information regarding DIMM memory designs using ECC, refer to the Intel 440BX AGPset design guide.
2. MAB[13,10] signals are not inverted because these address bits are used to define various SDRAM commands.

4.1.2 SDRAM Signal Connectivity

The DRAM expansion socket is a 144-pin SO-DIMM. Table 5 identifies the SDRAM signals and the corresponding SO-DIMM pins. Table 6 identifies the 82443BX SDRAM signals and the corresponding onboard SDRAM signals.

Table 5. SDRAM Signals and Corresponding SO-DIMM Pins

Signal Name	SO-DIMM Pin
MAB[11]#	106
MAB[12]#	70, 110
MAB[13]	72, 112

Table 6. 82443BX SDRAM Signals and Corresponding Onboard SDRAM Signals

Signal Name	SDRAM Component Pin
MAB[11]#	A13/BA0
MAB[12]#	A12/BA1
MAB[13]	A11

4.1.3 Pin Groups

The 82443BX has multiple copies of many of the signals interfacing to memory. However, the recommendations in this design guide are based on only a single copy of the memory signals. See “Single Set DRAM Interface” on page 32 for more information. The interface consists of the following pins:

Multiple copies:

MAA[13:0], MAB[12:11,9:0]# and MAB[13, 10]
CSA[7:0]#, CSB[7:0]#
SRASA#, SRASB#
SCASA#, SCASB#
WEA#, WEB#
DQMA[7:0], DQMB[5:1]

Single copies:

CKE[5:0] (for three SODIMM configuration)
MD[63:0]
MECC[7:0]
GCKE (for four DIMM configuration)
FENA (FET switch control for four DIMM configuration)

Two CS# lines are provided per row. These are functionally equivalent. The extra copy is provided for loading reasons. The two SRAS#, SCAS# and WE# pins are also functionally equivalent and each copy drives two rows of DRAM. Most pins use programmable strength output buffers. When a row contains 16-Mbit SDRAMs, MAA11 and MAB11# function as Bank Select lines. When a row contains 64-Mbit SDRAMs, MAA[12:11], MAB[12:11] function as Bank Addresses

(BA[1:0], or Bank Selects). When the design does not support ECC, you may leave MECC[7:0] unconnected. When the design supports ECC, perform simulations to determine which buffer strength is needed for loading requirements. This may require a BIOS change.

4.1.4 Single Set DRAM Interface

The following two sections explain which signals are used in embedded platforms. Note that MAB[13,10] are not active low because these address bits are used to define various SDRAM commands.

4.1.4.1 SDRAM

Single copies used:

MAB[12:11,9:0]# and MAB[13,10]
MD[63:0]
MECC[7:0]
CSA[5:0]#
DQMA[7:0]
CKE[5:0]
SRASA#
SCASA#
WEA#

4.2 General SDRAM Layout Guidelines

The following list identifies the SDRAM layout guidelines:

1. To obtain the most advantageous system electronics board layout, byte lanes may be swapped. Bits within a byte lane may also be swapped. However, bits between byte lanes may not be swapped.
2. A system electronics board nominal trace width should have an impedance of 55 Ω ± 10%. Impedance of a nominal trace width is a key parameter specified to board fabricators. Typically, nominal trace width is constrained by design density, the substrate material, and the board fabrication process. Common trace widths are 4 mils, 5 mils, and 6 mils.
3. All resistors should have a maximum ± 5% tolerance.
4. Populate the furthest SO-DIMM first to avoid stub reflections.
5. Any onboard memory should replace the furthest SO-DIMM socket.
6. Place onboard DRAM and SO-DIMM connectors as near as possible to each other.
7. CKBF-M should be powered by V_3 (the 3.3 V rail power supply which remains on during Suspend).

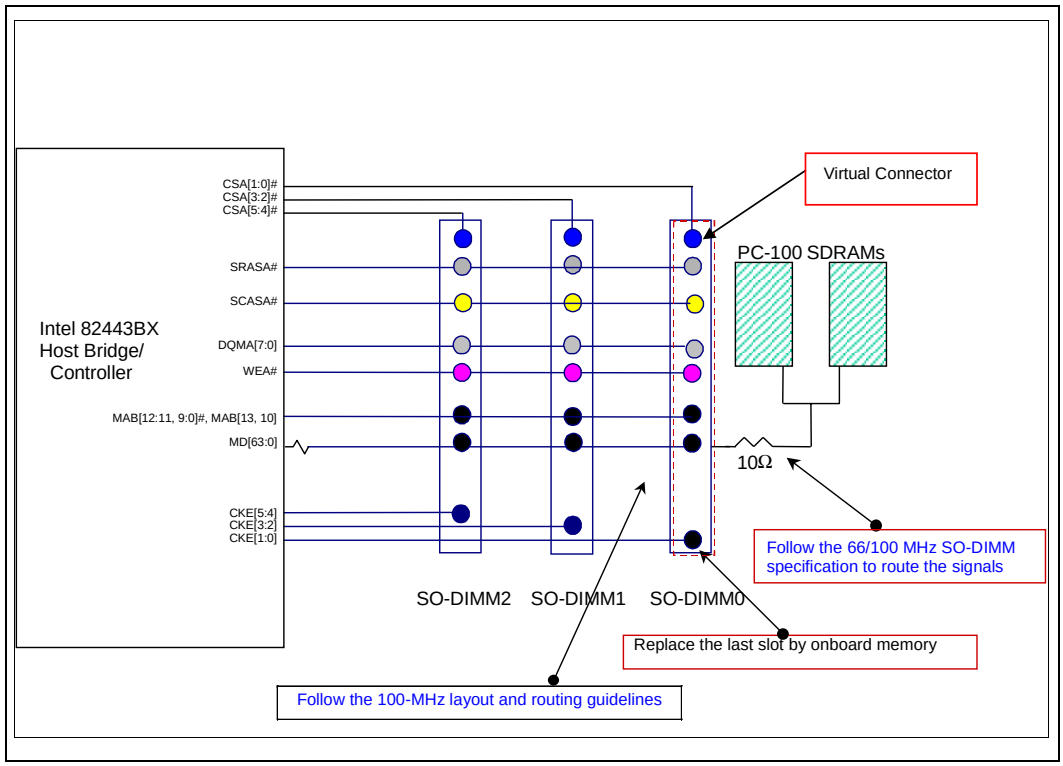
4.2.1 SO-DIMM Connection to SDRAM

Guidelines for the following memory configurations are provided: three SO-DIMM sockets, two SO-DIMM sockets, or two SO-DIMM sockets with onboard memory. For memory configurations with onboard memory, the onboard memory routing may be treated as a third SO-DIMM. For

example, the onboard memory is routed to a place on the board where a third SO-DIMM connector would otherwise be placed. In this document, the space is identified as a ‘virtual’ SO-DIMM connector. See Figure 8 for more detail.

The ‘virtual’ SO-DIMM connector is not a physical component but a design reference point (placeholder).

Figure 8. SDRAM Connections



4.3 Trace Lengths for Three or Two SO-DIMM Designs

The figures and tables below show the topology, and provide the minimum and maximum trace lengths to the SODIMM connector pads for each signal group in a three or two SO-DIMM design.

4.3.1 MD[63:0] Signals

Figure 9 and Table 7 list the three SO-DIMM socket trace lengths and illustrates the corresponding topology.

Figure 9. MD[63:0] Topology, Three SO-DIMM Sockets

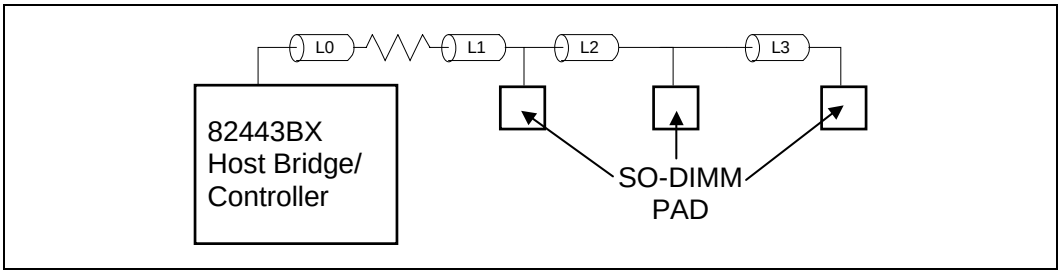


Table 7. MD[63:0] Topology, Three SO-DIMM Sockets - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	0.0 in	1.00 in
L0+L1	1.1 in	N/A
L2+L3	0.0 in	2.75 in
L0+L1+L2+L3	1.1 in	4.25 in

Figure 10 and Table 8 list the two SO-DIMM socket trace lengths and illustrates the corresponding topology.

Figure 10. MD[63:0] Topology, Two SO-DIMM Sockets

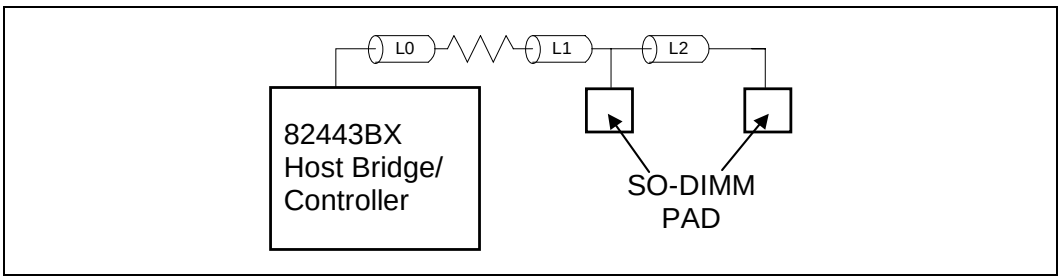


Table 8. MD[63:0] Topology, Two SO-DIMM Sockets - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	0.0 in	1.0 in
L0+L1	1.1 in	N/A
L0+L1+L2	1.1 in	6.0 in

4.3.2 DQMA[7:0] Signals

Figure 11 and Table 9 list the three SO-DIMM trace lengths and illustrates the corresponding topology.

Figure 11. DQMA [7:0] Topology, Three SO-DIMM Sockets

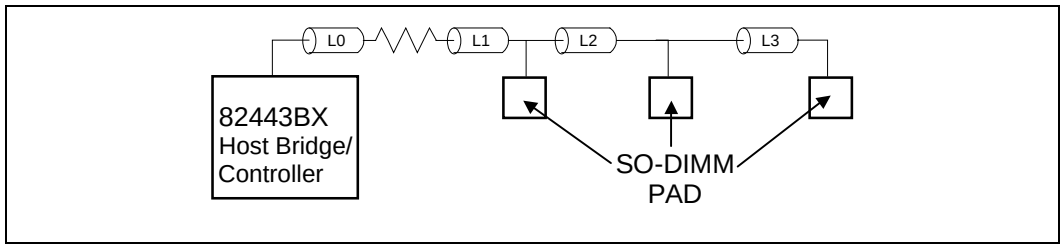


Table 9. DQMA [7:0] Topology, Three SO-DIMM Sockets, Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	N/A
L0+L1+L2	1.0	4.0

Figure 12 and Table 10 list the two SO-DIMM trace lengths and illustrates the corresponding topology.

Figure 12. DQMA [7:0] Topology, Two SO-DIMM Sockets

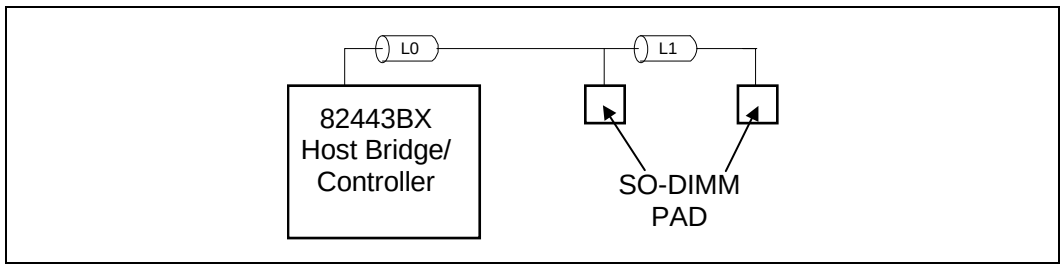


Table 10. DQMA [7:0] Topology, Two SO-DIMM Sockets - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	N/A
L0+L1	1.0	6.0

4.3.3 Chip Select Signals - CSA[5:0]

Figure 13 and Table 11 list the Chip Select signals and illustrates the corresponding topology.

Figure 13. CSA [5:0] Topology

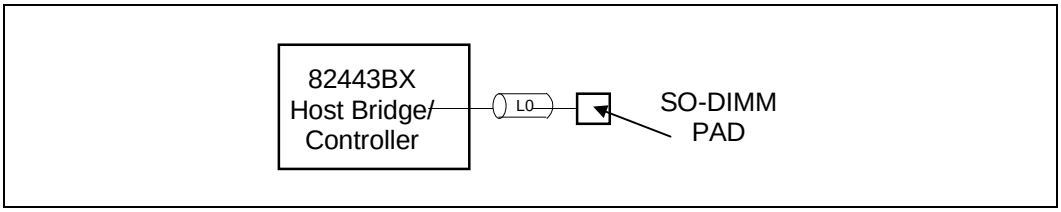


Table 11. CSA[5:0] Topology - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	6.0

4.3.4 Clock Enable Signals - CKE[5:0]

Figure 14 and Table 12 list the Clock Enable signals and illustrates the corresponding topology.

Figure 14. CKE[5:0] Topology

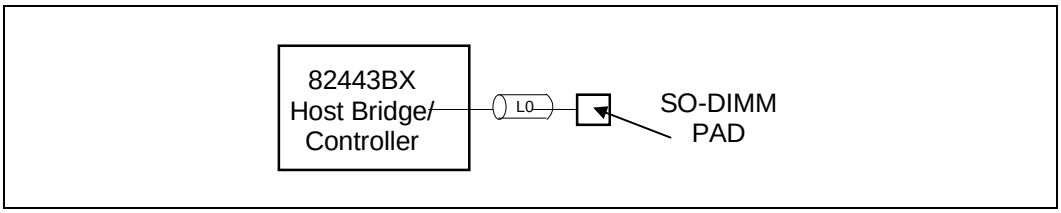


Table 12. CKE[5:0] Topology - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	6.0

4.3.5 Command Signals - MAB[13:0]x, WEA#, SRASA#, and SCASA

Figure 15 and Table 13 list the three SO-DIMM trace lengths for the command signals and illustrate the corresponding topology.

Figure 15. Command Signals Topology, Three SO-DIMM

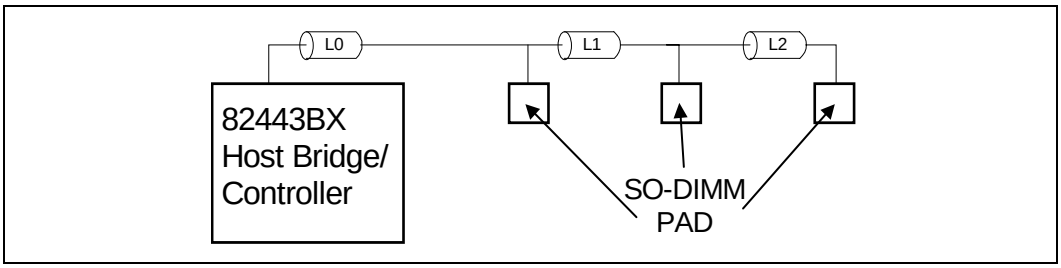


Table 13. Command Signals Topology, Three SO-DIMM - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	N/A
L0+L1+L2	1.0	6.0

Figure 16 and Table 14 list the two SO-DIMM trace lengths for the command signals and illustrates the corresponding topology.

Figure 16. Command Signals Topology, Two SO-DIMM

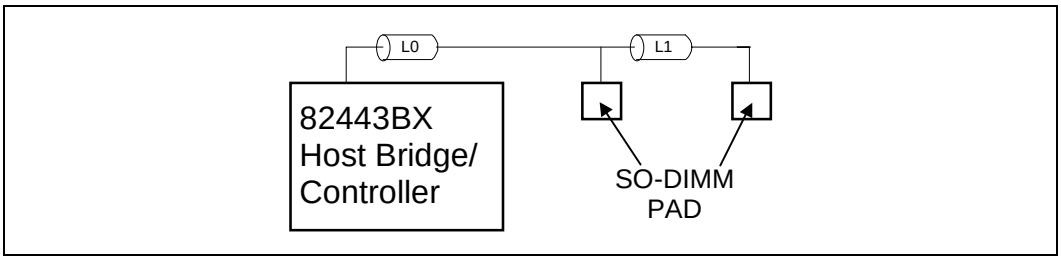


Table 14. Command Signals Topology, Two SO-DIMM - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	N/A
L0+L1	1.0	6.0

4.4 SODIMM DRAM Organization

The 144-pin SODIMM (one inch height) has a maximum capacity of eight devices and provides the following configuration possibilities (see Table 15) for SDRAM.

Table 15. SODIMM DRAM Organization

Technology	SODIMM Organization	Component Organization	Devices per Row	Mbyte per SODIMM
16 Mbit	1 M x 64 / S	1 M x 16	4	8 Mbyte
	2 M x 64 / D	1 M x 16	4	16 Mbyte
	2 M x 64 / S	2 M x 8	8	16 Mbyte
64 Mbit	2 M x 64 / S	2 M x 32	2	16 Mbyte
	4 M x 64 / D	2 M x 32	2	32 Mbyte
	4 M x 64 / S	4 M x 16	4	32 Mbyte
	8 M x 64 / D	4 M x 16	4	64 Mbyte
	8 M x 64 / S	8 M x 8	8	64 Mbyte
128 Mbit	16 M x 64 /S	8 M x 16	4	128 Mbyte

NOTE: ‘S’ denotes single-sided SODIMMs; ‘D’ denotes double-sided SODIMMs.

4.4.1 SDRAM System Examples

Table 16 lists five system examples. Each example is based on using three SODIMM sockets or one on-board DRAM and two SODIMM sockets. The terms used in Table 16 are defined below:

144 SODIMM: Number of SODIMM sockets plus on-board DRAM
Row: RAS[5:0]# or CS[5:0]# connection.
Technology: DRAM technology 16 Mbit, 64 Mbit, 128 Mbit
Density/Width: DRAM configuration 16 Mbit: 2 M x 8, or 1 M x 16
64 Mbit: 8 M x 8, 4 M x16, or 2 M x 32
128 Mbit: 8 M x 16, or 16 M x 8
Devices/Row: Number of DRAM components per row.

Table 16. SDRAM System Examples

144 SODIMM	Row	Technology	Density x Width	# Devices/Row	Mbytes per SODIMM
Example #1					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	16 Mbit	1 M x 16	4	8 Mbytes
	2	16 Mbit	1 M x 16	4	8 Mbytes
#3	3	16 Mbit	2 M x 8	8	16 Mbytes
Total	4			24	48 Mbytes
Example #2					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	16 Mbit	2 M x 8	8	16 Mbytes
#3	2	16 Mbit	2 M x 8	8	16 Mbytes
Total	3			24	48 Mbytes
Example #3					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	64 Mbit	8 M x 8	8	64 Mbytes
#3	2	64 Mbit	4 M x 16	4	32 Mbytes
Total	3			20	112 Mbytes
Example #4					
#1 or on-board	0	64 Mbit	8 M x 8	8	64 Mbytes
#2	1	64 Mbit	8 M x 8	8	64 Mbytes
#3	2	64 Mbit	8 M x 8	8	64 Mbytes
Total	3			24	192 Mbytes
Example #5					
#1 or on-board	0	128 Mbit	8 M x 16	4	64 Mbytes
	1	128 Mbit	8 M x 16	4	64 Mbytes
#2	2	128 Mbit	8 M x 16	4	64 Mbytes
	3	128 Mbit	8 M x 16	4	64 Mbytes
#3	4	128 Mbit	8 M x 16	4	64 Mbytes
	5	128 Mbit	8 M x 16	4	64 Mbytes
Total	6			24	384 Mbytes

4.5 SO-DIMM Placement Options

There are many ways to place the SO-DIMMs on the system electronics. The following diagrams illustrate a few of the possibilities. The dotted outline indicates the SO-DIMM socket is on the other side of the board. In all the configurations, the last SO-DIMM (SODIMM0) slot may be replaced by on-board memory.

Figure 17. Three SO-DIMM Slots on One Side (First Two Back-to-Back)

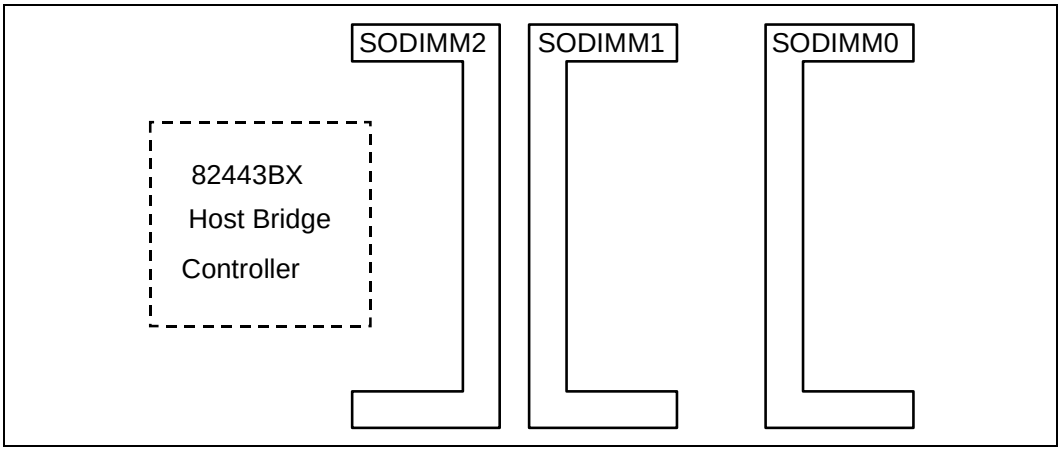


Figure 18. Two SO-DIMM Slots Back-to-Back, Third Slot on the Other Side

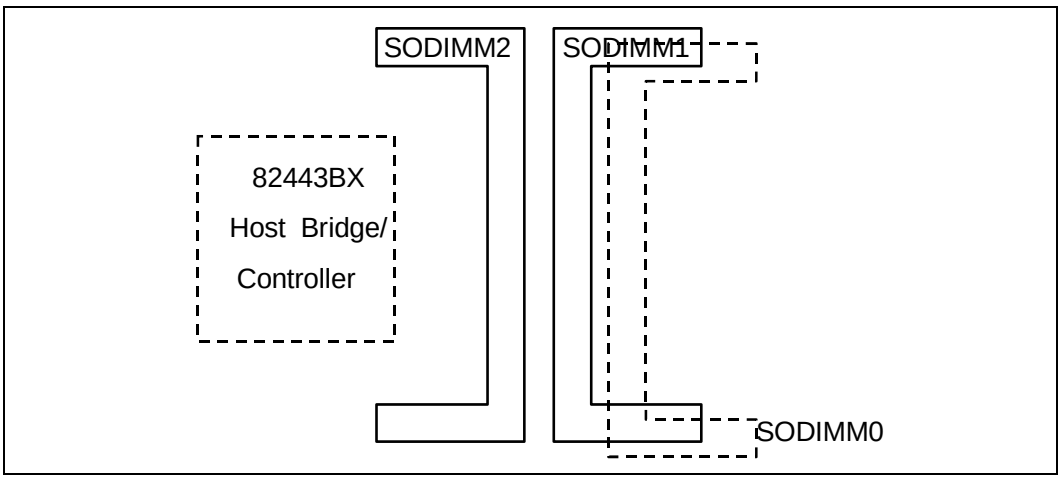


Figure 19. Two SO-DIMM Slots on One Side, Third Slot on the Other Side

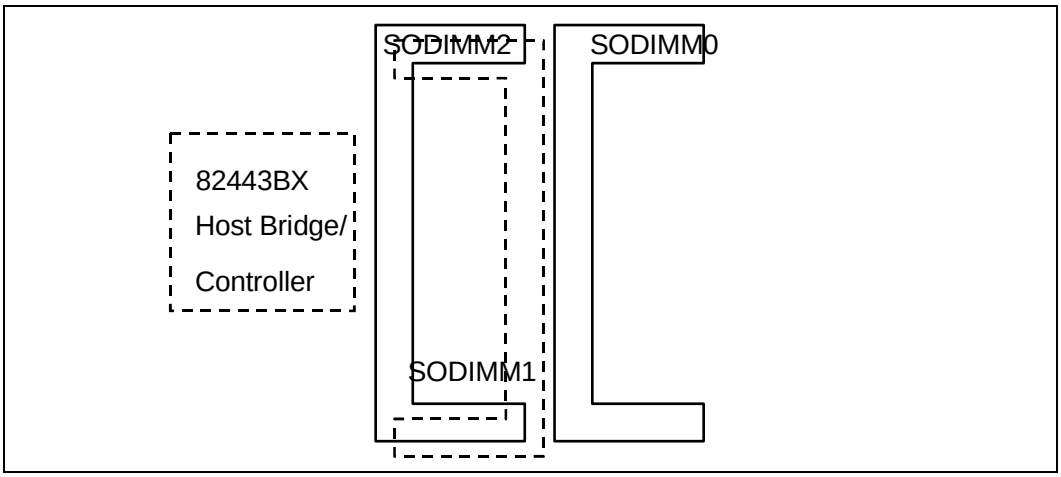
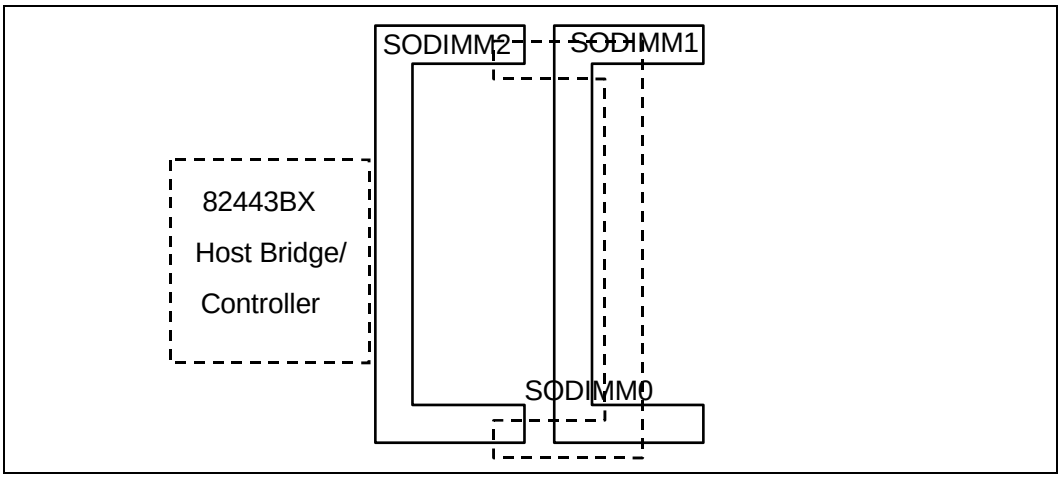


Figure 20. Two SO-DIMM Slots on One Side, Third Slot on the Other Side (Alternate Method)



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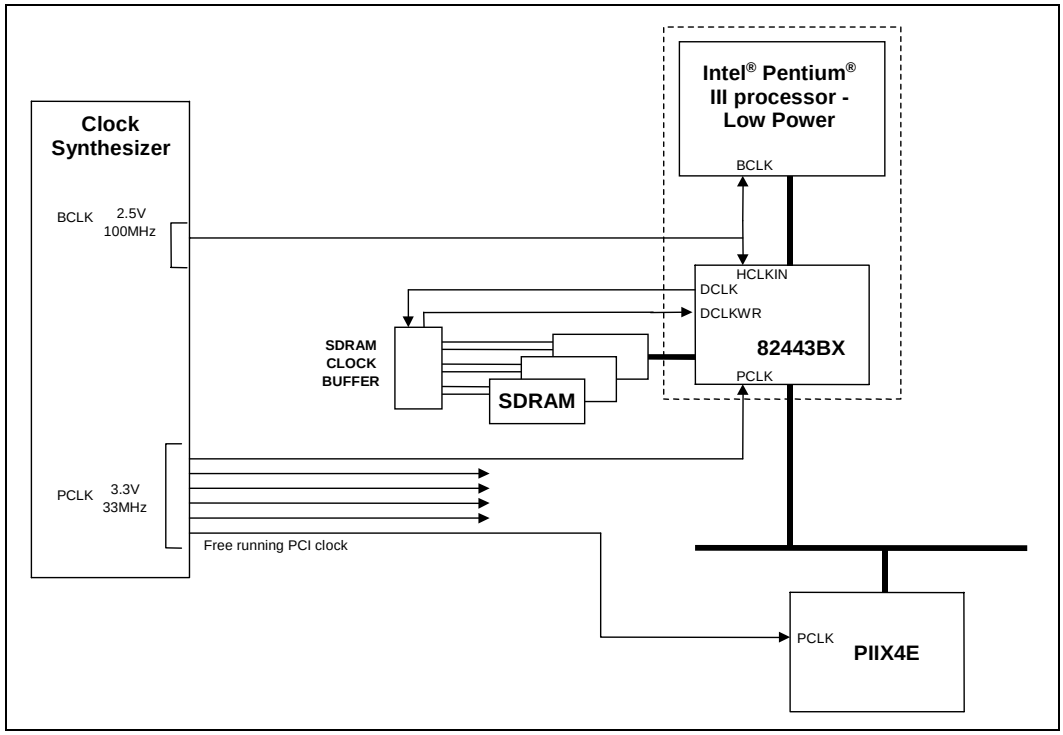
5.0 Clocking Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order in which signals are routed will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing the high-speed bus signals first. Either order may be used, as long as the guidelines listed here are followed. When the guidelines listed here are not followed, it is very important to simulate the design. Even when the guidelines are followed, it is recommended that you simulate signals for proper signal integrity, flight time and cross talk.

5.1 Clocking System Overview

This section provides guidelines and application information for clock layout in a Pentium® III processor – Low Power/440BX AGPset system. These guidelines are based on the HCLK, PCICLK and SDRAMCLK requirements and should be implemented along with the application instructions supplied by your clock chip vendor. Figure 21 shows the clock synthesizer connection to the processor, 82443BX, PIIX4E, and SDRAM.

Figure 21. Clock Connections to the Intel® Pentium® III Processor — Low Power and 440BX Chipset



5.2 Clock Synthesizer Pinout and Specifications

A clock synthesizer that meets the *CK97 Clock Synthesizer Design Guidelines* (order number 243867) will meet the requirement for a Pentium III processor – Low Power/440BX AGPset-based system. Table 22 lists clock vendors that provide clock synthesizers which meet the *CK97 Clock Synthesizer Design Guidelines*.

Note: The CK100-M compatible clock synthesizer operates in multi-voltage mode. The processor clocks operate at 100 MHz at 2.5 V, and the PCI clocks operate at 33 MHz at 3.3 V. The CKBF-M compatible clock buffer provides clocks for SDRAM operating at 100 MHz at 3.3 V. See Figure 22 and Figure 23 for more details.

Figure 22. Pinout for CK100-M Compatible Clock Synthesizer

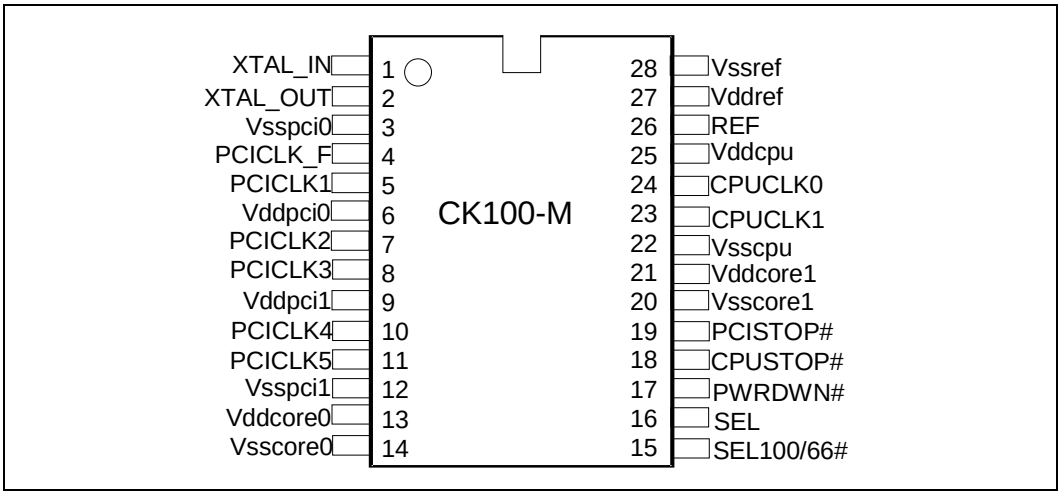
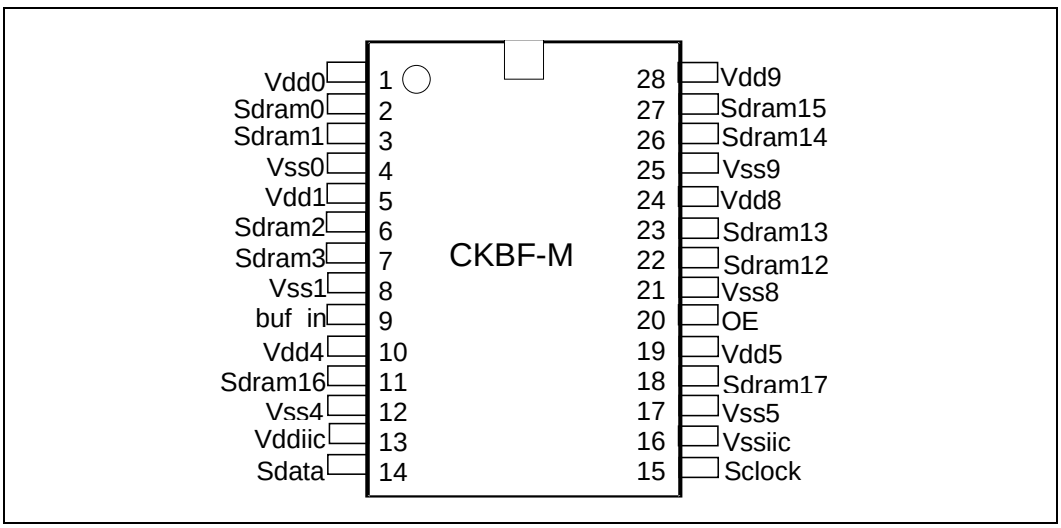


Figure 23. Pinout for CKBF-M Compatible Clock Buffer



5.3 Timing Guidelines

Figure 24 shows a simplified clocking layout for the timing specifications. See Table 17 for the clock skews.

Figure 24. Timing Specifications Layout

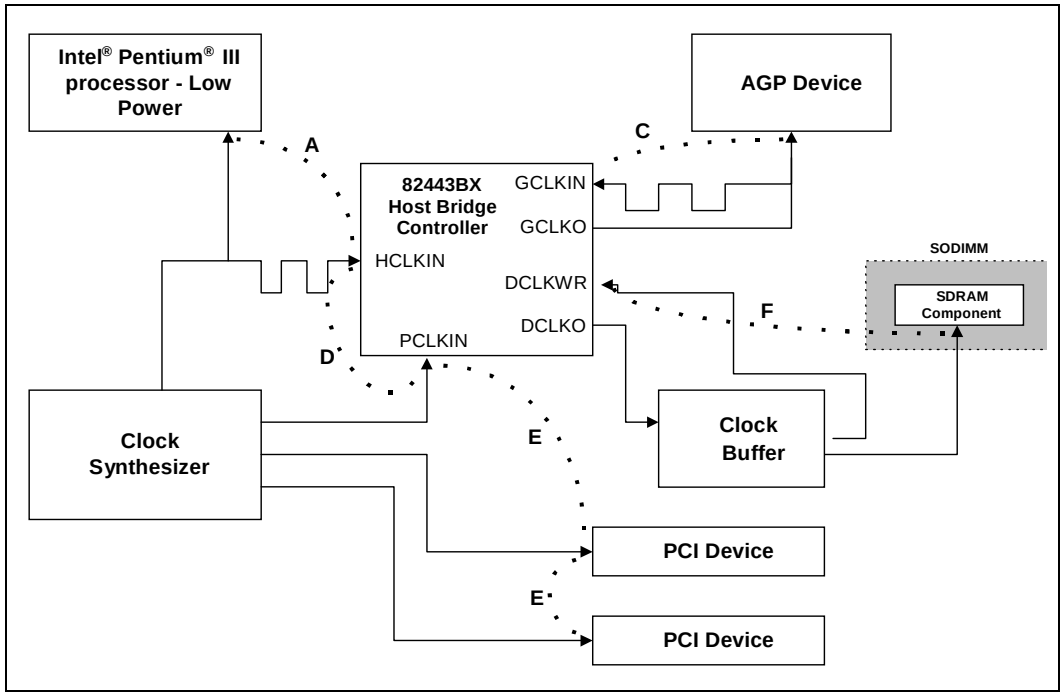


Table 17. Timing Specifications for Maximum and Minimum Clock Skews

Symbol	Description	CK100-M pin to pin	Boards	Total
A	CPU (BCLK) to 82443BX (HCLKIN) skew	0 ps (max) [1] 0 ps (min) [1]	250 ps (max) [3] -250 ps (min) [3]	250 ps (max) [3] -250 ps (min) [3]
C	AGP device (GCLK) to 82443BX (HCLKIN) skew	N/A	100 ps (max) -100 ps (min)	100 ps (max) - 100 ps (min)
D	82443BX (HCLKIN) to PCI (PCLK) skew	4.0 ns (max.) [2] 1.5 ns (min.)	1.0 ns (max.) 0 ns (min.)	5.0 ns (max.) 1.5 ns (min.)
E	PCI (PCLK) to PCI (PCLK) skew	500 ps (max) -500 ps (min)	1.5 ns (max) -1.5 ns (min)	2.0 ns (max) - 2.0 ns (min)
F	DCLKWR to SDRAM (SCLK) skew	250 ps (max) -250 ps (min)	380 ps (max) [4] -380 ps (min) [4]	630 ps (max) - 630 ps (min)

NOTES:
1. In a Pentium® III processor – Low Power based design, use the same clock output pin for both the 82443BX HCLK input and the processor clock input in a 'T' signal trace configuration.
2. The 82443BX PCICLK input should lag its HCLK input by a minimum of 1.5 ns to a maximum of 4.0 ns at the pins of the CK100-M device. An integrated buffer will offer the best control over these output to output drive skews.
3. The total allowable CPU(BCLK) to 82443BX(HCLKIN) skew for the Pentium III processor – Low Power is ±250 ps.
4. This skew allowance includes ±280 ps for I/O capacitance and SODIMM routing variation. Motherboards should be designed to allow for no more than ±100 ps contribution to the total skew.

Note: .Clock period, jitter, offset and skew are measured on the rising edge of the clock signals at 1.25 V for the 2.5 V clocks and at 1.5 V for the 3.3 V clocks.

5.4 Host Clock Layout Guidelines

The following list provides Host Clock guidelines for a Pentium III processor – Low Power design:

1. The trunk trace length (from clock driver output pin to T-split) may range from 2.0 inches to 4.5 inches, with the entire length at an 8-mil trace width. (8-mil trace width on a layer where a 4-mil trace is nominally 55 Ω)
2. Clocks must be routed on the same layer internally to contain EMI. Space all other signals at least 2 W from clock traces.
3. A series resistor at the clock driver is 22Ω ±5% tolerance, placed as near to the driver pin as possible (up to 0.5 inches). Intel recommends that the clock series resistors not be placed in the R-packs to allow individual tunability if necessary.
4. Minimize the vias on all clock traces.
5. Do not allow the clock traces to cross a plane split.

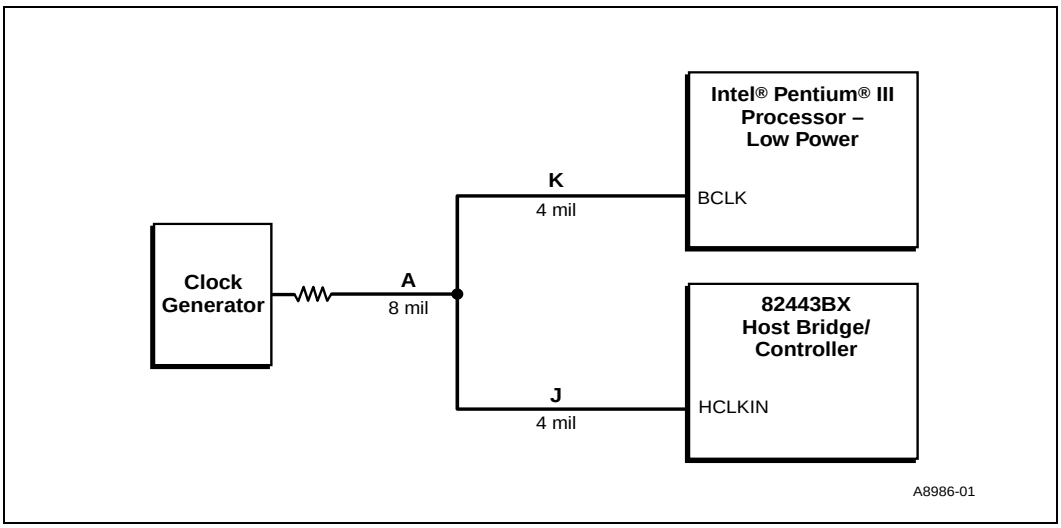
Table 18. Host Clock Trace Length Guidelines

Variable	Trace Width	Minimum Trace Length (inches)	Maximum Trace Length (inches)	Resistor
A	8 mil	2.0 in	4.5 in	22 Ω ± 5%
J	4 mil	1.25 in	1.35 in	N/A
K	4 mil	J + 0.876 in	J + 0.878 in	N/A

NOTE: Table 18 refers to a board where characteristic impedance is nominally 55 Ω ± 10% at 4 mils.

The Host Clock should be routed in an unbalanced ‘T’ topology. Route the branches of the ‘T’ in 4-mil wide traces and route the trunk of the ‘T’ in an 8-mil wide trace. Place the trunk of the ‘T’ such that the Pentium III processor – Low Power branch is equal to the BX branch + 0.877.

Figure 25. Host Clock Topology



5.5 SDRAM Clock Layout Guidelines

This section defines the clock lengths and series termination for 100-MHz SDRAM clocks.

5.5.1 General Clocking Guidelines

The goal of the SDRAM clock guidelines is to route all SDRAM clock signals as near to the same length as possible, not deviating more than 0.2 inches from maximum to minimum.

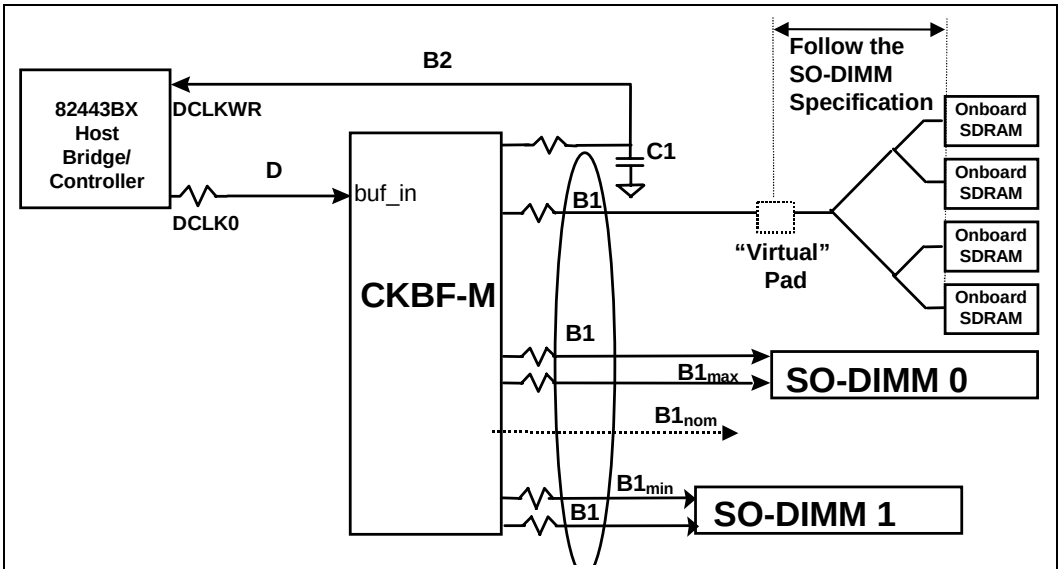
The following list provides design considerations for the SDRAM clocks.

1. Series termination resistors are required. Place them as close to the driver pin as possible (within 1 inch).
2. Route all SDRAM clocks and DCLKWR on the same internal layer to provide better trace delay consistency as well as EMI containment.
3. A system electronics board nominal trace width should have an impedance of 55 Ω ± 10%. Impedance of a nominal trace width is a key parameter specified to board fabricators. Typically, nominal trace width is constrained by design density, the substrate material, and the board fabrication process. Common trace widths are 4 mils, 5 mils, and 6 mils.
4. Minimize the use of vias in clock signals.
5. All clocks should have 1:2 width-to-spacing ratio.
6. A zero delay buffer should not be used in place of the CKBF-M.

5.5.2 SDRAM Clock Layout Guidelines

Figure 26 shows the SDRAM clock layout guidelines and Table 19 provides the measurement values.

Figure 26. Clocking Layout Diagram



NOTES:
1. B1 represents memory SDRAM clock signals.
2. $B1_{max}$ represents the "Maximum" SDRAM clock trace length.
3. $B1_{nom}$ represents an imaginary "Nominal" SDRAM clock trace length.
4. $B1_{min}$ represents the "Minimum" SDRAM clock trace length.

Intel recommends the following guidelines for SDRAM clock trace length design. The terms used in Figure 26 are mathematically defined as follows:

1. SDRAM clock trace lengths should not differ in length from maximum to minimum by more than 0.2 inches. This means that the longest SDRAM clock trace length ($B1_{max}$) minus the shortest SDRAM clock trace length ($B1_{min}$) should be within 0.2 inches of each other; $B1_{max} - B1_{min} \leq 0.2$ inches.
2. $B1_{nom}$ is an imaginary target nominal SDRAM clock trace length that is centered in length between the maximum and the minimum SDRAM clock lengths. This is defined as:

$$B1_{nom} = B1_{min} + \frac{B1_{max} - B1_{min}}{2}$$

3. B1= $B1_{nom}$ ± 0.1 inches (maximum = $B1_{nom}$ + 0.1 in, minimum = $B1_{nom}$ - 0.1 in).
4. B2 = DCLKWR = $B1_{nom}$ + 2.5 inches ± 0.1 inches (maximum = $B1_{nom}$ + 2.6 in, minimum = $B1_{nom}$ + 2.4 in).

Table 19. SDRAM Clocks and DCLK Trace Lengths

Variable	Trace Zo	Trace Length (min)		Trace Length (max)		Resistor
$B1_{nom}$	N/A	0.0 in	0.0 mm	4.0 in	101.6 mm	N/A
B1	55 Ω ± 10%	$B1_{nom}$ - 0.1 in	$B1_{nom}$ - 2.5 mm	$B1_{nom}$ + 0.1 in	$B1_{nom}$ + 2.5 mm	10 Ω ± 5%
B2	55 Ω ± 10%	$B1_{nom}$ + 2.4 in	$B1_{nom}$ + 61 mm	$B1_{nom}$ + 2.6 in	$B1_{nom}$ + 66.0 mm	22 Ω ± 5%
D	55 Ω ± 10%	0.0 in	0.0 mm	4.0 in	101.6 mm	18 Ω ± 5%
C1	15 pF ± 5%	Use a 0603 package size with an NPO or C0G dielectric and place it within 0.2 inches of the resistor. Route from the resistor pad through the capacitor pad and then into the via going into the system electronics board.				

5.5.3 DCLKWR Layout Guidelines

Intel recommends that a capacitor be added to the system electronics on the DCLKWR signal. Notebook designers should use a capacitor value that will minimize the skew between the SDRAM clocks and the Intel 82443BX component. The capacitor should be placed no more than 0.2 inches from the 22-Ω series dampening resistor. Intel recommends using the topology shown in Figure 27. This allows the capacitor to be removed from a design without creating an open-ended stub on DCLKWR. See Table 20 for section tolerances.

1. Series matching resistors are required. Placement: As near to the driver pin as possible (within 1 inch).
2. Route all clocks on internal layers to provide better trace delay consistency as well as EMI containment.
3. Board impedance should be 55 Ω ± 10%.
4. Minimize the use of vias in clock signals.
5. All clocks should have 1:2 width to spacing ratio.

Figure 27. DCLKWR (Figure 16, Variable B2) Guidelines

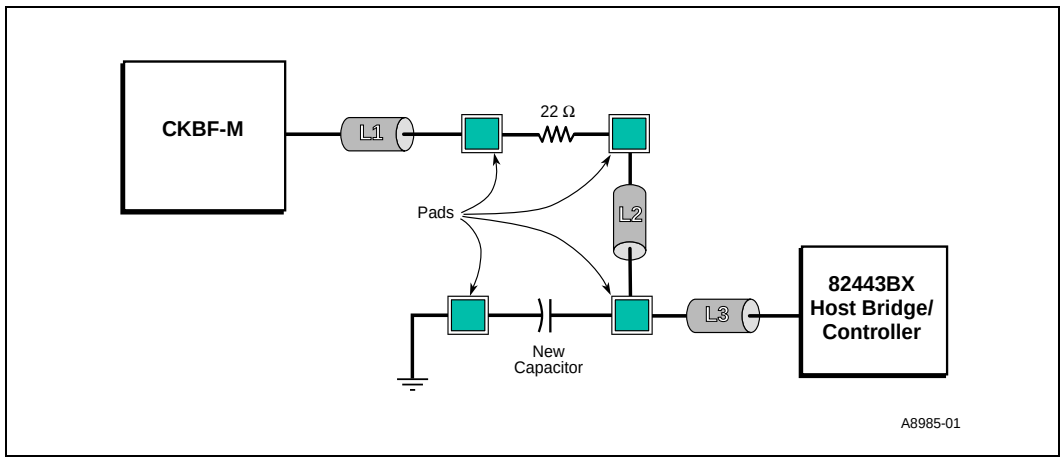


Table 20. DCLKWR Guidelines - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L1	0.0	1.0
L2	0.0	0.2
L3	N/A	N/A
L1+L2+L3	$B1_{nom}$ +2.4 in	$B1_{nom}$ +2.6 in

5.6 PCI/AGP Clock Layout Guidelines

Note: Figure 28 assumes AGP and PCI devices are 'down' on the motherboard and not on a connector. When designing a board that will use connectors to add AGP or PCI devices, be sure to take into account the trace length already routed on the AGP or PCI card. PCI cards have a PCI CLK trace length of 2.5 inches. AGP cards have an AGP CLK trace length of approximately 3.3 inches.

Figure 28. PCI and AGP Clocking Layout

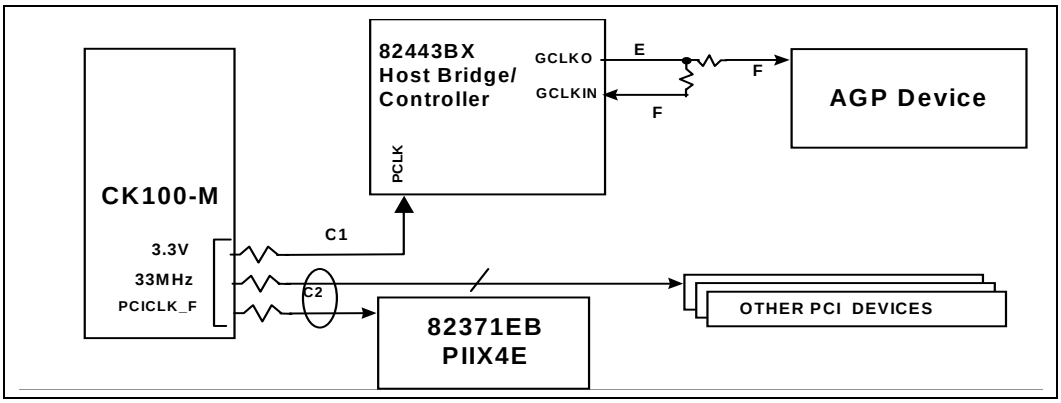


Table 21. PCI and AGP Clock Trace Length

Variable	Trace Width	Minimum Trace Length	Maximum Trace Length	Tolerance	Resistor Value
C_1	5 mil	A+J	A+J+4 inch (A+J+101.6 mm)		33 Ω ± 5%
C_2	5 mil	C_1	C_1	± 4.5 inch (± 114.3mm)	33 Ω ± 5%
E	10 mil	0 inch (0 mm)	1 inch (25.4 mm)		None
F	5 mil	0 inch (0 mm)	8.5 inch (215.9 mm)		18 Ω ± 5%

NOTE: Tolerance refers to the allowed difference in length between multiple traces sharing the same variable name.

5.7 Clock Vendors

This vendor list is provided as a service to our customers for reference only. The inclusion of this list should not be considered a recommendation or product endorsement by Intel Corporation.

Table 22. Clock Vendors

Vendor Name	Address
International Microcircuits, Inc.	525 Los Coches Street Milpitas, CA 95035 (408) 263-6300 http://www.imicorp.com
Integrated Circuit Systems, Inc.	1271 Parkmoor Avenue San Jose, CA 95126-3448 (408) 925-9493 http://www.icst.com
Cypress Semiconductor	12020 113th Ave. Northeast Kirkland, WA 98034 (425) 398-3400 http://www.cypress.com

6.0 82443BX AGP Interface Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. Even when the guidelines are followed, it is recommended that you simulate as many signals as possible for proper signal integrity and cross talk. See Section 7.3.5 for AGP pull-up requirements. See Section 5.0, “Clocking Guidelines” on page 43 for AGP clocking information.

6.1 Layout and Routing Guidelines

For the definition of AGP interface functionality (protocols, rules and signaling mechanisms, and the platform level aspects of AGP functionality), refer to the latest *AGP Interface Specification* and *AGP Platform* design guide. This document focuses only on specific 440BX platform recommendations for the AGP interface.

Throughout this section the term ‘data’ refers to G_AD[31:0], G_C/BE[3:0]# and SBA[7:0]. The term ‘strobe’ refers to AD_STB[B:A] and SB_STB. When the term ‘data’ is used, it is referring to one of three groups of data as indicated in Table 23. When the term ‘strobe’ is used it is referring to one of the three strobes as it relates to the data in its associated group.

Table 23. Data and Associated Strobe

Data	Associated Strobe
G_AD[15:0] and G_C/BE[1:0]#	AD_STBA
G_AD[31:16] and G_C/BE[3:2]#	AD_STBB
SBA[7:0]	SB_STB

6.1.1 On-board AGP Compliant Device Layout Guidelines

Longer trace lengths require a greater amount of spacing between traces in order to reduce crosstalk. When using 1:2 spacing, maximum trace length of data lines is 9.5 inches. The line length mismatch is 0.5 inches. The strobe is the longest trace of the group. This restricts the maximum trace length of data lines to less than 4.5 inches for a 1:1 trace spacing. The strobe requires a 1:2 trace spacing. Trace length guidelines given in this section do not reflect signal integrity and EMI. It is recommended that you simulate the routes to ensure that signal quality requirements are met. See Figure 29 for the AGP compliant device layout guidelines and Figure 30 for signal layout recommendations.

Figure 29. On-board AGP Compliant Device Layout Guidelines

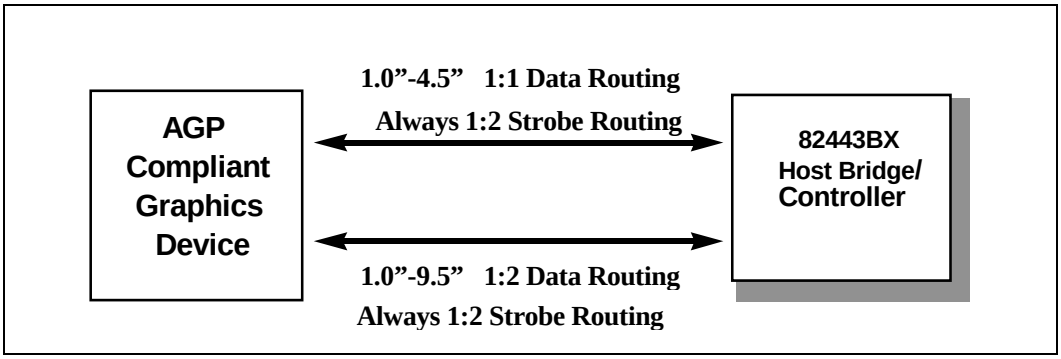
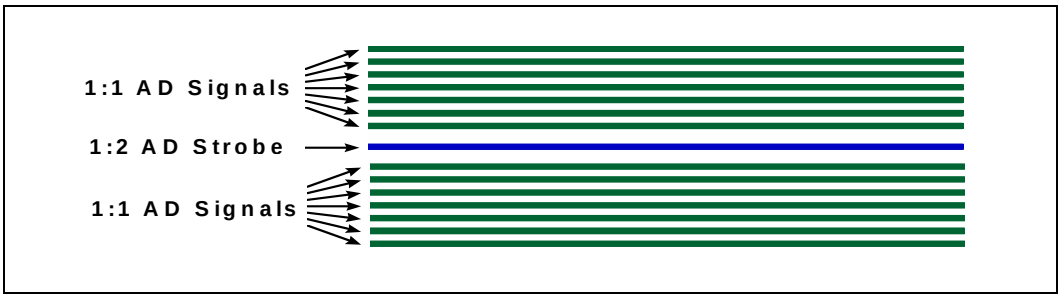


Figure 30. Signal Layout Recommendations



6.1.1.1 Data and Strobe Signal Routing Recommendations

Table 24. Motherboard Recommendations

Width:Space	Trace	Line Length	Line Length Matching
1:1(Data)/1:2(Strobe)	Data /Strobe	1.0 in < line length < 4.5 in	0.5 in, strobe longest trace
1:2	Data/Strobe	1.0 in < line length < 9.5 in	0.5 in, strobe longest trace

The line length mismatch must be less than 0.5 inches and the strobe must be the longest signal of the group. For example, if the strobe is at 4.0 inches, the data line may be from 3.5 to 4.0 inches in length. It is best to reduce the line length mismatch wherever possible to ensure added margin. The strobe is always required to have 1:2 trace spacing. It is also best to separate the traces by as much as possible in order to reduce the amount of trace-to-trace coupling.

Note: Under certain layouts, crosstalk and ground bounce may be observed on the AD_STB signals of the AGP interface. Although Intel has not observed system failures due to this issue, noise margin has been improved by enhancing the AGP buffers on the 82443BX. For new designs, additional margin may be obtained by following AGP layout guidelines.

6.1.1.2 Control Signal Routing Recommendations

Some of the control signals require pull-up resistors to be installed on the motherboard. Pull-up resistors should be discrete resistors, since resistor packs will need longer stub lengths and may violate timing requirements. The stub length to these pull-up resistors must be controlled. The maximum stub length on a strobe trace is < 0.1 inch. The maximum stub trace length on all other traces is < 0.5 inch. See Table 25 for control signal line length recommendations. For pull-up recommendations, see "AGP Interface Signals" on page 66.

Table 25. Control Signal Line Length Recommendations

Width:Space	Board	Trace	Line Length	Pull-up Stub Length
1:1	Motherboard	Control Signals	1.0 in < line length < 8.5 in	< 0.5 in (Strobes < 0.1 in)
1:2	Motherboard	Control Signals	1.0 in < line length < 10.0 in	< 0.5 in (Strobes < 0.1 in)

6.2 ACPI Compliance Requirements

Based on the Advanced Configuration and Power Interface (ACPI) specification, the AGP graphics device must be ACPI compliant and must implement its self power management circuitry, such as self clock-gating and an idle bus detection mechanism to reduce power. However, in a Pentium® III processor-based platform the AGP device clock is a derivative of the host clock.

When the host clock stops (C3 state - Deep Sleep), the AGP clock also stops. An AGP_BUSY# protocol solves this instantaneous AGP stop clock problem. The AGP graphics device must signal the operating system or the south bridge that it is currently busy and the AGP clock should not be stopped.

The AGP device internally protects its core logic to ensure that an illegal clock will not corrupt the AGP device state. This protection gates the internal clock nets used for the device's logic from the time STP_AGP# is asserted until it is deasserted. The STP_AGP# signal is an indication that the AGP clock will not be valid for much longer and should be gated off for protection. STP_AGP# should be connected to the PIIX4E's SUS_STAT1# signal.

The AGP_BUSY# signal indicates that the graphics controller requires the GCLK to be running. This signal should be connected to one of the PIIX4E's PCIREQ# pins. When the PCIREQ# pin must be shared, it may be logically ORed with one of the PIIX4E's PCIREQ# inputs. AGP_BUSY# is an open-drain signal from the graphics device and requires a 10 KΩ pull-up resistor.

AGP_SUSPEND# is for AGP devices that support Suspend mode. The AGP_SUSPEND# signal may be connected to the PIIX4E's SUSB# signal.

6.3 AGP IDSEL Routing

An AGP compliant master is composed of a PCI compliant target interface and an AGP compliant master interface. (Optionally the device may also include a PCI compliant master interface when required.) When used in a PCI mode of operation, the AGP device must provide an external IDSEL that is connected to AD16. When the AGP device is designed for exclusive operation on the AGP interface the device does not have an external IDSEL pin, therefore IDSEL does not need to be routed.

7.0 Design Guideline Checklists

Design checklists provided in this section are intended to be used for schematic reviews of the Pentium® III processor – Low Power/440BX AGPset platform designs. The checklists do not represent the only way to design a system, but do provide recommendations. The system designer should examine the checklist items for correctness. Additional design considerations are also provided.

7.1 Resistor Values

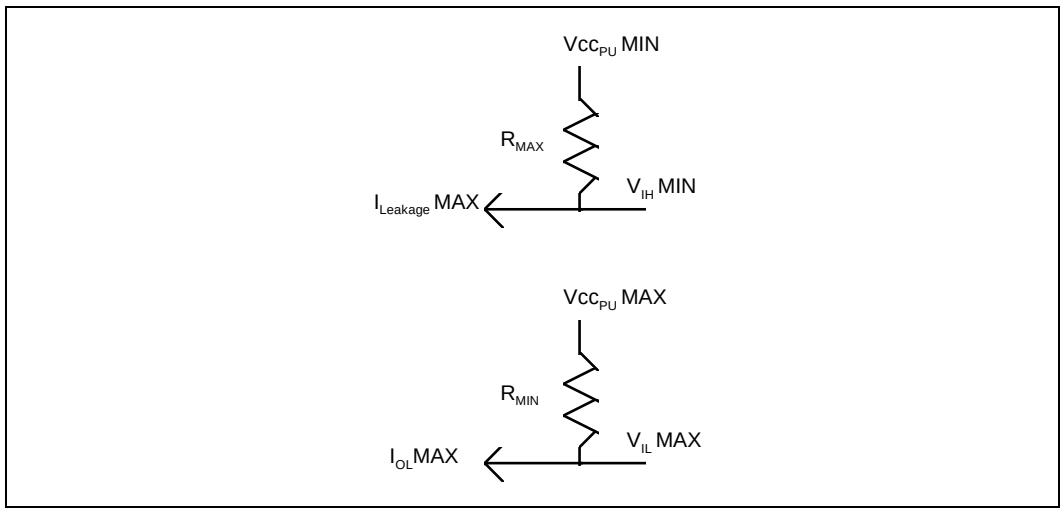
Pull-up and pull-down resister values are system dependent. The appropriate value for your system may be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum and maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination may include cost concerns, commonality considerations, manufacturing issues, specification and other considerations. See Figure 31 for an example for a pull-up resistor configuration.

A simplistic DC calculation for a pull-up value is:

$R_{MAX} = (Vcc_{PU}\ MIN - V_{IH}\ MIN) / I_{Leakage}\ MAX$

$R_{MIN} = (Vcc_{PU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$

Figure 31. Pull-up Resistor Example



7.2 Pentium III Processor – Low Power Design Checklist

7.2.1 GTL+ Signals

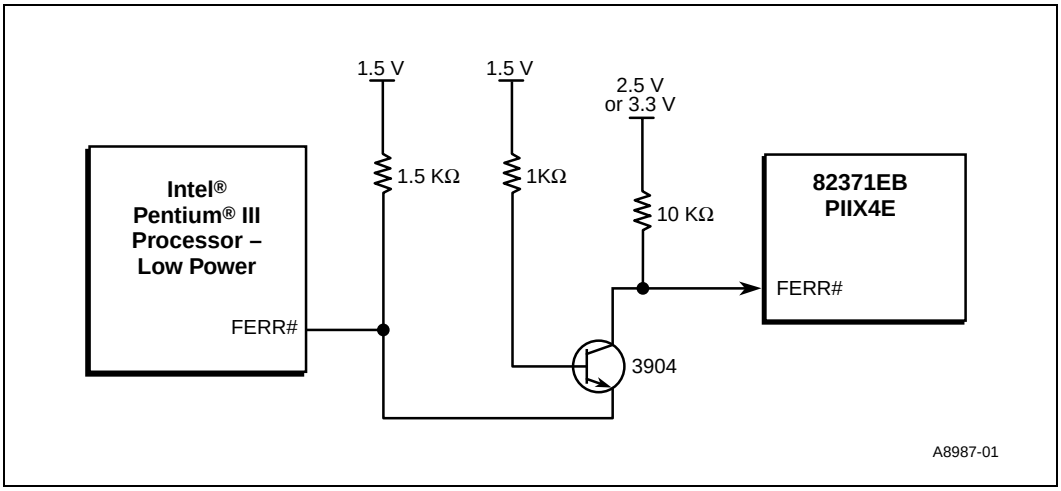
Table 26. GTL+ Signals

	CPU Pin	Pin Connection
	A[35:3]#	A[31:3]#: Connect to 82443BX. A[35:32]#: NO CONNECT
	ADS#	Connect to 82443BX
	AERR#	NO CONNECT
	AP[1:0]#	NO CONNECT
	BERR#	NO CONNECT
	BINIT#	NO CONNECT
	BNR#	Connect to 82443BX
	BP[3:2]#	NO CONNECT
	BPM[1:0]#	NO CONNECT
	BPRI#	Connect to 82443BX
	BREQ0#	Connect to 82443BX pin BREQ0#. Optional 10 Ω pull-down to Vss.
	D[63:0]#	Connect to 82443BX
	DBSY#	Connect to 82443BX
	DEFER#	Connect to 82443BX
	DEP[7:0]	NO CONNECT
	DRDY#	Connect to 82443BX
	HIT#	Connect to 82443BX
	HITM#	Connect to 82443BX
	LOCK#	Connect to 82443BX
	REQ[4:0]#	Connect to 82443BX
	RESET#	Terminate to V_{CCT} with 56.2 Ω 1% resistor / Connect to 82443BX
	RP#	NO CONNECT
	RS[2:0]#	Connect to 82443BX
	RSP#	NO CONNECT
	TRDY#	Connect to 82443BX

7.2.2 CMOS Signals

- FERR# is an open-drain signal from the Pentium III processor – Low Power and must be pulled-up to VCCT with a 1.5 KΩ resistor. In addition to this pull-up, external glue logic is needed to convert the 1.5 V signal to 2.5 V or 3.3 V. Figure 32 illustrates the implementation of the glue logic.

Figure 32. External Glue Logic



- CMOS open-drain signals should have maximum trace length of five inches. When CMOS undershoot specifications are not met with the recommended pull-ups, stronger pull-ups may be required. Please see the *Intel® Pentium® III Processor — Low Power Datasheet* (order number 273500) for details on CMOS signal specifications.
- Intel recommends that the PWRGOOD signal from the power supply not be connected directly to logic on the board, without first going through a Schmitt trigger type circuitry to square-off and maintain the signal integrity.
- To enable Quick Start state: Pull-up SLP# pin on the processor to VCCT with a 1.5 KΩ resistor, pull-up MAB10 on 443BX to 3 V with a 10 KΩ resistor, leave SLP# on PIIX4 unconnected.

Table 27. CMOS Signals

	CPU Pin	Pin Connection
	A20M#	1.5 KΩ pull-up to VCCT. Connect to PIIX4E.
	FERR#	1.5 KΩ pull-up to VCCT. Connect to PIIX4E. For an example of level conversion logic see Figure 32, “External Glue Logic” on page 59
	FLUSH#	1.5 KΩ pull-up to VCCT if not used.
	IERR#	1.5 KΩ pull-up to VCCT. Connect to error logic. No connect if not used.
	IGNNE#	1.5 KΩ pull-up to VCCT. Connect to PIIX4E.
	INIT#	1 KΩ pull-up to VCCT. Connect to PIIX4E.
	LINT[1]/NMI	1.5 KΩ pull-up to VCCT. Connect to PIIX4E.
	LINT[0]/INTR	1.5 KΩ pull-up to VCCT. Connect to PIIX4E.
	PICD[1:0]	1 KΩ pull-down to Vss.
	PREQ#	1.5 KΩ pull-up to VCCT. Connect to ITP.
	PWRGOOD	1.5 KΩ pull-up to 2.5 V. Connect to power sense logic
	SLP#	1.5 KΩ pull-up to V_{CCT}. Connect to PIIX4E.
	SMI#	270 Ω pull-up to V_{CCT}. Connect to PIIX4E.
	STPCLK#	680 Ω pull-up to V_{CCT}. Connect to PIIX4E.

7.2.3 TAP Signals

	CPU Pin	Pin Connection
	PRDY#	56.2 Ω 1% pull up to VCCT, 240 Ω series resistor to ITP connector
	TCK	1 KΩ pull-up to VCCT. 47 Ω series resistor to ITP connector; 1 KΩ pull-down if not used.
	TDO	150 Ω pull-up to VCCT. Connect to ITP. No connect if not used
	TDI	150 Ω pull-up to VCCT. Connect to ITP; 1 KΩ pull-down if not used.
	TMS	1 KΩ pull-up to VCCT. 47 Ω series resistor to ITP connector; 1 KΩ pull-down if not used.
	TRST#	1 KΩ pull-down to Vss. Connect to ITP

7.2.4 Clock Signals

- Ensure that the clock generation logic is at a 2.5-V level (BCLK and PICCLK) and at a 1.5 V level (TCK) into the Pentium III processor – Low Power.
- Use discrete resistors for the BCLK signals from the CK100M. Do not mix HCLK, and PCLK signals coming from the CK100M device in resistor packs.

Table 28. Clock Signals

	CPU Pin	Pin Connection
	BCLK	Connect to 82443BX HCLKIN and CK100M with 22 Ω series resistor at the CK100M device. See Section 5.0 for clock routing guidelines.
	PICCLK	1 KΩ pull-down to Vss.

7.2.5 Miscellaneous Signals

Table 29. Miscellaneous Signals

	CPU Pin	Pin Connection
	BSEL0	1 KΩ pull-up to V_{CCT}.
	BSEL1	1 KΩ pull-down to Vss.
	EDGCTRLP	110 Ω 1% Pull-down to Vss.
	GHI#	NO CONNECT
	RTTIMPEDP	56.2 Ω 1% pull-down to Vss
	TESTHI	1 KΩ pull-up to V_{CCT}.
	TESTLO[2:1]	1 KΩ pull-down to Vss.
	THERMDC	NO CONNECT if not used. Otherwise connect to thermal sensor.
	THERMDA	NO CONNECT if not used. Otherwise connect to thermal sensor.
	VID[4:0]	For Voltage Regulator's (VR) that do not contain internal pull-ups use a 10 KΩ pull-up to 5 V; Connect to VR.

7.2.6 Power Pins

Table 30. Power Pins

	CPU Pin	Pin Connection
	CLKREF	Board divider on $V_{CC2.5}$ or $V_{CC3.3}$ to create 1.25 V reference with a 0.1 µF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. Do not use V_{CCT} as source voltage for this reference.
	CMOSREF	Board divider on $V_{CC2.5}$ or $V_{CC3.3}$ to create 1.0 V reference with a 0.1 uF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. Do not use V_{CCT} as source voltage for this reference.
	PLL[2:1]	Typically a 4.7 µH inductor in series with V_{CCT} is connected to PLL1 then through a series 33µF capacitor to PLL2. Refer to the *Intel® Pentium® III Processor – Low Power Datasheet* (order number 273500) for more information.
	V_{CC}	Connect to Voltage Regulator output. For decoupling guidelines see Section 7.2.8
	V_{CCT}	Connect to Voltage Regulator output. For decoupling guidelines see Section 7.2.8
	V_{REF}	$V_{REF} = 2/3\ V_{CCT}$. Create with voltage divider made up of 1 KΩ ± 1% and 2 KΩ ± 1% resistors connected to V_{CCT}. Decouple with 3 (min) 0.1 µF high freq. caps close to processor.
	V_{SS}	Tie to GND

7.2.7 NO CONNECT Pins

Table 31. NO CONNECT Pins

	CPU Pin	Pin Connection
	NC	The following pins must be left as NO CONNECTS: A15, A16, A17, C14, D8, D14, D16, E15, G2, G4, G5, G18, H3, H4, H5, J5, M4, M5, P3, P4, R2, AA5, AA17, AA19, AC3, AC17, AC20, AD15, AD20
	RSVD	The following pins must be left as NO CONNECTS: AB19

7.2.8 Processor Decoupling Requirements

For a processor operating at 700 MHz and above, the following decoupling is recommended. The processor core power plane (V_{CC}) should have 15 0.68 µF 0603 ceramic capacitors (using X7R dielectric for thermal reasons) placed directly under the package using two vias for power and two vias for ground to reduce the trace inductance. Also to minimize inductance, traces to those vias should be 22mils (in width) from the capacitor pads to match the via-pad size (assuming 22-mil pad size). Twenty-four 2.2 µF 0805, X5R mid frequency decoupling capacitors should be placed around the die as close to the die as flex solution allows.

The system bus buffer power plane (V_{CCT}) should have twenty (20) 0.1-µF high frequency decoupling capacitors around the die.

For a processor operating at 650 MHz and below, the following decoupling is recommended. The processor core power plan (V_{CC}) should have twelve (12) 0.1 µF high frequency decoupling capacitors placed underneath the die and twenty seven (27) 0.1 µF mid frequency decoupling capacitors placed around the die as close to the die (< 0.8 inch away) as flex solution allows. The system bus buffer power plane (V_{CCT}) should have 15 0.1-µF high frequency decoupling capacitors no further than 0.25 inch away from the V_{CCT} vias (balls).

7.3 82443BX Design Checklist

7.3.1 Host Interface Signals

Table 32. Host Interface Signals

	82443BX Pin	Pin Connection
	CPURST#	Connect to CPU and ITP (240 Ω series resistor)
	HA[31:3]#	Connect to CPU
	HD[63:0]#	Connect to CPU
	ADS#	Connect to CPU
	BNR#	Connect to CPU
	BPRI#	Connect to CPU
	BREQ0#	Connect to CPU. Optional, leave as No Connect if CPU BREQ0# pin is pulled to Vss with a 10 Ω resistor
	DBSY#	Connect to CPU
	DEFER#	Connect to CPU
	DRDY#	Connect to CPU
	HIT#	Connect to CPU
	HITM#	Connect to CPU
	HLOCK#	Connect to CPU
	HREQ[4:0]	Connect to CPU
	HTRDY#	Connect to CPU
	RS[2:0]#	Connect to CPU

7.3.2 DRAM (SO-DIMM) Interface Signals

- For standard DIMM SDRAM interface signal guidelines refer to the Intel® 440BX AGPset Design Guide.
- MD[63:0] should have 10 Ω series termination resistors for SO-DIMM designs.
- Clock signals from the CKBF-M to each SO-DIMM should have 10 Ω series termination resistors.
- A zero delay buffer should not be used in place of the CKBF-M.

Table 33. DRAM (SO-DIMM) Interface Signals

	82443BX Pin	Pin Connection
	RASA[5:0]# /CSA[5:0]#	Connect two CSA[5:0]# signals to each SO-DIMM.
	CASA[7:0]# /DQMA[7:0]#	Connect DQMA[7:0]# to each SO-DIMM.
	CKE[5:0]	Connect two CKE signals to each SO-DIMM
	SRASA#	Connect SRASA# to each SO-DIMM
	SCASA#	Connect SCASA# to each SO-DIMM
	MAB[0:9]#	Connect to associated address pin of SO-DIMM
	MAB10	Connect to A10 pin of SO-DIMM
	MAB11#	Connect to SO-DIMM pin #106
	MAB12#	Connect to SO-DIMM pin #70, #110
	MAB13	Connect to SO-DIMM pin #72, #112
	WEA#	Connect WEA# to each SO-DIMM
	MD[63:0]	10 Ω series resistor. Connect MD[63:0] to each SO-DIMM
	MECC[7:0]	10 Ω series resistor. Connect MECC[7:0] to each SODIMM. Leave as No Connect if not used.

7.3.3 PCI Interface Signals

- The 82443BX supports up to five PCI masters with its REQ[4:0]#/GNT[4:0]# pairs. The PCI bus supports up to ten PCI loads. The 82443BX and the PIIX4E each represent one load; other PCI components soldered on the motherboard add one load each; and each PCI connector adds approximately two loads. A design with four PCI slots and no motherboard devices uses all available PCI loads. When all five REQ[4:0]#/GNT[4:0]# pairs are used, simulation is required to ensure that the *PCI Bus Specification*, Rev. 2.1, timings are met.

Table 34. PCI Interface Signals

	82443BX Pin	Pin Connection
	AD[31:0]	Connect to PCI Slots and PIIX4E.
	DEVSEL#	2.7 K Ω pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect to PCI Slots and PIIX4E.
	FRAME#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect to PCI Slots and PIIX4E.
	IRDY#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect to PCI Slots and PIIX4E.
	C/BE[3:0]#	Connect to PCI Slots and PIIX4E.
	PAR	Connect to PCI Slots and PIIX4E.
	PLOCK#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect to PCI Slots.
	TRDY#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect to PCI Slots and PIIX4E.
	SERR#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect to PCI Slots and PIIX4E.
	STOP#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect to PCI Slots and PIIX4E.

7.3.4 PCI Sideband Signals

Table 35. PCI Sideband Signals

	82443BX Pin	Pin Connection
	PHOLD#	10 KΩ pull-up to 3.3 V. Connect to PIIX4E.
	PHLDA#	10 KΩ pull-up to 3.3 V. Connect to PIIX4E.
	WSC#	NO CONNECT
	PREQ[4:0]	10 KΩ pull-up to 3.3 V. Connect to PCI Slots.
	PGNT[4:0]	10 KΩ pull-up to 3.3 V. Connect to PCI Slots.

7.3.5 AGP Interface Signals

- To disable AGP, tie MAB9# high using a 10 KΩ pull-up to 3.3 V, connect GCLKO to GCLKIN through an 18 Ω resistor, and ground AGPREF. When AGP is properly disabled, all AGP signals are tri-stated and isolated; no termination is needed.

Table 36. AGP Interface Signals

	82443BX Pin	Pin Connection
	PIPE#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	SBA[7:0]	Connect to AGP connector.
	RBF#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	ST[2:0]	Connect to AGP connector.
	ADSTB_A	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	ADSTB_B	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	SBSTB	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	GFRAME#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	GIRDY#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	GTRDY#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	GSTOP#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	GDEVSEL#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	GREQ#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	GGNT#	8.2 KΩ pull-up to 3.3 V. Connect to AGP connector.
	GAD[31:0]	Connect to AGP connector.
	GC/BE[3:0]#	Connect to AGP connector.
	GPAR	100 KΩ pull-down to Vss. Pull-down not required if the AGP device uses GFRAME# only.

7.3.6 Clocks, Resets, and Miscellaneous Signals

- See Section 5.0 for clock routing guidelines.

Table 37. Clocks, Resets, and Miscellaneous Signals

	82443BX Pin	Pin Connection
	HCLKIN	Connect to CPU BCLK and CK100M through 22 Ω series resistor at CK100M device
	PCLKIN	Connect to CK100M through 33 Ω series resistor.
	DCLKO	Connect to CKBFM through 18 Ω series resistor placed next to 82443BX.
	DCLKWR	22 Ω series termination at CKBFM. ‘T’ at the 22 Ω resistor with 15 pF cap to Vss.
	PCIRST#	Connect to AGP, PCI, and PIIX4E. 33 Ω series resistor next to PIIX4E.
	GCLKIN	Connect to GCLKO through 18 Ω series resistor.
	GCLKO	Connect to AGP device through 18 Ω series resistor.
	CRESET#	NO CONNECT. Optional connect to bus ratio logic for qualification processors.
	TESTIN#	8.2 KΩ pull-up to 3.3 V. May be removed if validation permits.

7.3.7 Power Management Interface

Table 38. Power Management Interface

	82443BX Pin	Pin Connection
	CLKRUN#	When not connected to PIIX4E, pull-down with a 100 Ω resistor at both the 82443BX and PIIX4E. Otherwise, pull-up to 3.3 V with a 10 KΩ and connect to PIIX4E.
	SUSTAT#	10 KΩ pull-up to 3.3 V. Connect to PIIX4E SUS_STAT1# pin for POS implementation.
	BXPWROK	Connect to processor PWRGOOD pin through voltage conversion logic. Connect to PIIX4E PWROK pin.

7.3.8 Reference Pins

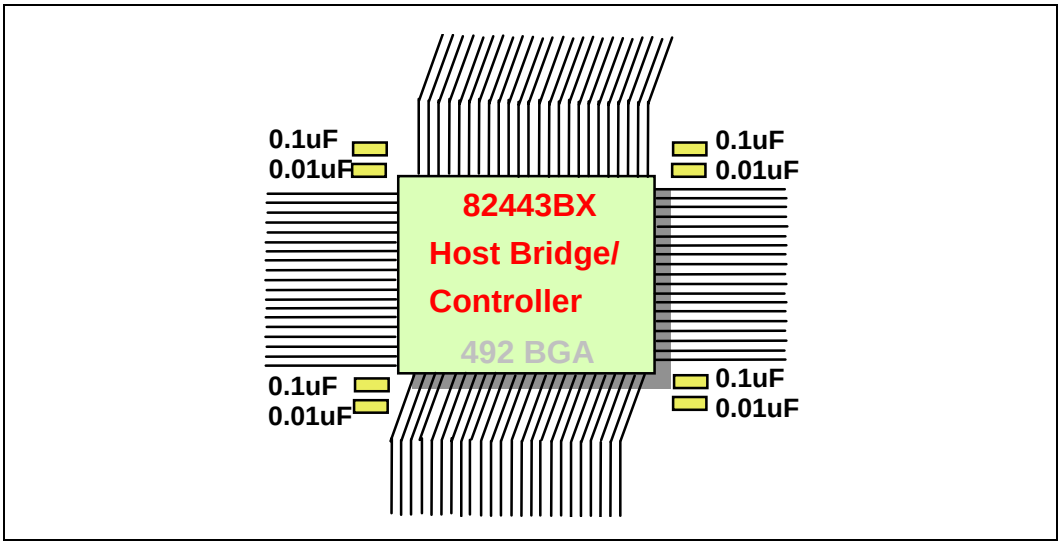
Table 39. Reference Pins

	82443BX Pin	Pin Connection
	GTLREF[B:A]	GTLREF = 2/3 VCCT. Use voltage divider with R1 = 1.0 KΩ 1%, and R2 = 2.0 KΩ 1%. Place two 0.1uF caps next to 82443BX
	VTT[B:A]	Tie to VCCT voltage plane.
	VCC	Power pin at 3.3 V.
	VSS	Tie to GND.
	REF5V	For a 5 V tolerant PCI bus connect to 5 V through a 1 KΩ resistor. See Section 8.2.1 for voltage sequencing requirements. For non-5 V tolerant PCI connect directly to 3.3 V.
	AGPREF	AGPREF = (2/5)3.3 V. Use a voltage divider with R1 = 3.48 KΩ 1% and R2 = 2.32 KΩ 1%. Place 0.1uF cap next to 82443BX. When disabling AGP, tie to ground.

7.3.9 82443BX Decoupling Guidelines

Decoupling caps should be placed at the corners of the 82443BX (BGA Package). A minimum of four 0.1 µF and four 0.01 µF are recommended. The system bus, AGP, PCI, and DRAM interface may break out from the BGA package on all four sides. Additional caps will also help reduce EMI and cross-talk. Refer to Figure 33 for decoupling topology.

Figure 33. 82443BX Decoupling



7.3.10 82443BX Strapping Options

- Highlighted strapping options shown below are required for this platform.
- Internal resistors are 50 KΩ pull-up or pull-down.
- Use external resistors of 10 KΩ to configure modes.
- Strapping option pull-ups should be to 3.3 V.

Table 40. 82443BX Strapping Options

Pin Name	Function	Low	High	Internal Resistor	Status Register
MAB12#	Host Frequency Select	66 MHz	100 MHz	Pull-down	NBXCFG[13]
MAB11#	In-Order Queue Depth Enable	1 (no pipelining)	4 (max)	Pull-up	NBXCFG[2]
MAB10	Quick Start Select	Stop Clock Mode	Quick Start Mode	Pull-down	PMCR[3]
MAB9#	AGP Disable	AGP Enabled	AGP Disabled	Pull-down	PMCR[1]
MAB7#	MM Configuration	Normal Operation	Tri-states certain Memory signals	Pull-down	DRAMC[5]
MAB6#	Host Bus Buffer Mode Select	Desktop GTL+	Low Power GTL+	Pull-down	None

7.4 82371EB (PIIX4E) Design Checklist

7.4.1 PCI Interface Signals

- For systems in which the PCIRST# signal is lightly loaded (< 50pF), place a 47 pF capacitor to Vss on this signal. The capacitor should be placed as close as possible to the PIIX4E.

Table 41. PCI Interface Signals

	PIIX4E Pin	Pin Connection
	AD[31:0]	Connect to PCI slots and 82443BX.
	C/BE#[3:0]	Connect to PCI slots and 82443BX.
	CLKRUN#	10 KΩ pull-up to 3.3 V. Connect to 82443BX. When not used, tie a 100 Ω pull-down at both the 82443BX and PIIX4E.
	DEVSEL#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect between 82443BX, PCI slots, and PIIX4E.
	FRAME#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect between 82443BX, PCI slots, and PIIX4E.
	IDSEL	100 Ω series resistor to AD18.
	IRDY#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect between 82443BX, PCI slots, and PIIX4E.
	PAR	Connect to PCI slots and 82443BX.
	PCIRST#	33 Ω series resistor next to PIIX4E. Connect to AGP, PCI, and 82443BX.
	PHOLD#	Connect to 82443BX. 10 KΩ pull-up to 3.3V.
	PHLDA#	Connect to 82443BX. 10 KΩ pull-up to 3.3V.
	SERR#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect between 82443BX, PCI slots, and PIIX4E.
	STOP#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect between 82443BX, PCI slots, and PIIX4E.
	TRDY#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect between 82443BX, PCI slots, and PIIX4E.

7.4.2 ISA/EIO Bus Interface Signals

- Recommendations below are for ISA implementation.
- When implementing Power On Suspend (POS) mode, ISA signals should be pulled up to 3.3 V. Otherwise use 5 V.

Note: This pull-up voltage is referred to V_{CCISA} in this checklist.

Table 42. ISA/EIO Bus Interface Signals

	PIIX4E Pin	Pin Connection
	AEN	Connect to SIO and ISA slots.
	BALE/GPO0	10K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	IOCHK# /GPI0	1K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	IOCHRDY	1K Ω pull-up to V_{CCISA}. Connect to ISA slots and Ultra I/O.
	IOCS16#	1K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	IOR#	10K Ω pull-up to V_{CCISA}. Connect to ISA slots, Ultra I/O, LM79.
	IOW#	10K Ω pull-up to V_{CCISA}. Connect to ISA slots, Ultra I/O, LM79.
	LA[23:17] /GPO[7:1]	10K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	MEMCS16#	1K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	MEMR#	10K Ω pull-up to V_{CCISA}. Connect to ISA slots and Flash.
	MEMW#	10K Ω pull-up to V_{CCISA}. Connect to ISA slots and Flash.
	REFRESH#	1K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	RSTDRV	Connect to Ultra I/O, ISA slots, and IDE (IDE through a Schmitt trigger).
	SA[19:0]	10K Ω pull-up to V_{CCISA}. Connect to ISA slots, Ultra I/O, Flash, LM79.
	SBHE#	10K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	SD[15:0]	10K Ω pull-up to V_{CCISA}. Connect to ISA slots, Ultra I/O, LM79.
	SMEMR#	10K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	SMEMW#	10K Ω pull-up to V_{CCISA}. Connect to ISA slots.
	ZEROWS#	1K Ω pull-up to V_{CCISA}. Connect to ISA slots.

7.4.3 X-Bus Interface Signals

Value of pull-up on A20GATE# and RCIN# could vary depending on SIO output type.

Table 43. X-Bus Interface Signals

	PIIX4E Pin	Pin Connection
	A20GATE#	10 KΩ pull-up to 3.3 V. Connect to SIO.
	BIOSCS#	Connect to Flash.
	KBCCS# /GPO26	NO CONNECT. When the KBCCS# signal is not used, this signal may be programmed to be a general-purpose output.
	MCCS#	NO CONNECT
	PCS[0:1]#	10 KΩ pull-up to 3.3 V. Connect to LM79. NO CONNECT if not used.
	RCIN#	10 KΩ pull-up to 3.3 V. Connect to SIO.
	RTCALE /GPO25	NO CONNECT. When the internal Real Time Clock is used, this signal may be programmed as a general-purpose output.
	RTCCS# /GPO24	NO CONNECT. When the internal Real Time Clock is used, this signal may be programmed as a general-purpose output.
	XDIR# /GPO22	Connect to SIO. NO CONNCET if not used. When the X-Bus not used, this signal may be programmed to be a general-purpose output.
	XOE# /GPO23	Connect to SIO. NO CONNECT if not used. When the X-Bus not used, this signal may be programmed to be a general-purpose output.

7.4.4 DMA Signals

Table 44. DMA Signals

	PIIX4E Pin	Pin Connection
	DACK[0,1,2,3]# DACK[5,6,7]#	Connect to ISA slots. DACK#[3:0] also connect to SIO.
	DREQ[0,1,2,3] DREQ[5,6,7]	Connect to ISA slots. 5.6 KΩ pull-down.
	REQ[A:C]# /GPI[2:4]	10 K Ω pull-up to 3.3 V. When the PC/PCI DMA request is not needed, these pins may be used as general-purpose inputs.
	GNT[A:C]# /GPO[9:11]	NO CONNECT. When the PC/PCI DMA acknowledge is not needed, these pins may be used as general-purpose outputs.
	TC	Connect to SIO and ISA slots.

7.4.5 Interrupt Controller/APIC Signals

Table 45. Interrupt Controller/APIC Signals

	PIIX4E Pin	Pin Connection
	APICACK# /GPO12	Connect to IOAPIC. When the external APIC is not used, this pin is a general-purpose output.
	APICCS# /GPO13	2.7 KΩ pull-up to 3.3 V. Connect to IOAPIC. When the external APIC is not used, this pin is a general-purpose output.
	APICREQ# /GPI5	10 KΩ pull-up to 3.3 V. Connect to IOAPIC. When the external APIC is not used, this pin is a general-purpose input.
	IRQ0/GPO14	Connect to INTIN2 of IOAPIC. When the external APIC is not used, this pin is a general-purpose output.
	IRQ1	10 KΩ pull-up to V_{CCISA}. Connect to ISA slots and Ultra I/O. Connect to IOAPIC.
	IRQ[3:7, 9:11] IRQ[14:15]	**IRQ[3:7, 9:11]** - 10 KΩ pull-up to V_{CCISA}. Connect to ISA slots and Ultra I/O. Connect to IOAPIC. **IRQ[14:15] -** 10 KΩ pull-up to V_{CCISA}. Connect to ISA slots, Ultra I/O and IDE. Connect to IOAPIC.
	IRQ8#/GPI6	10 KΩ pull-up to 3.3VSB. Connect to IOAPIC through tri-state buffer.
	IRQ9OUT /GPO29	Connect to IOAPIC. When the external APIC is not used, this pin is a general-purpose output.
	IRQ12/M	10 KΩ pull-up to V_{CCISA}. Connect to ISA slots and Ultra I/O. Connect to IOAPIC.
	PIRQ[A:D]#	2.7 KΩ pull-up to 5 V or 10 KΩ pull-up to 3.3 V. Connect between PCI slots and PIIX4E. PIRQ[A:B]# also go to AGP.
	SERIRQ /GPI7	10 KΩ pull-up to 3.3 V. When not using serial interrupts, this pin may be used as a genera purpose input.

7.4.6 CPU Interface Signals

Table 46. CPU Interface Signals

	PIIX4E Pin	Pin Connection
	A20M#	1.5 KΩ pull-up to VCCT.
	CPURST	NO CONNECT
	FERR#	Connect to voltage conversion logic as described in processor checklist.
	IGNNE#	1.5 KΩ pull-up to VCCT.
	INIT	1 KΩ pull-up to VCCT.
	INTR	1.5 KΩ pull-up to VCCT. Connect to IOAPIC.
	NMI	1.5 KΩ pull-up to VCCT.
	SLP#	1.5 KΩ pull-up to VCCT.
	SMI#	270 Ω pull-up to VCCT. Connect to IOAPIC.
	STPCLK#	680 Ω pull-up to VCCT.

7.4.7 Clocking Signals

- USB Clock – A 48 MHz clock with a duty cycle of better than 40%/60% should be fed into the PIIX4E's USB clock input, pin L3.
- The RTC capacitor value should be chosen to provide the manufacturer's specified load capacitance of the trace, socket (if used), and package which may vary from 0 pF to 8 pF. When choosing the value the following equation may be used:

  Specified Crystal Load = (Cap1*Cap2)/Cap1+Cap2) + parasitic capacitance

Table 47. Clocking Signals

	PIIX4E Pin	Pin Connection
	CLK48	Connect to 48 MHz clock through a 33 Ω series resistor. When not using USB, this may be connected to GND.
	PCICLK	Connect to CK100M through a 33 Ω series resistor.
	OSC	Connect to CK100M through a 33 Ω series resistor.
	RTCX1, RTCX2	Connect to 32.768 KHz crystal. Place capacitors on each side of crystal to Vss. For capacitor values see above.
	SUSCLK	NO CONNECT
	SYSCLK	Connect to LM79 and ISA slots. NO CONNECT if not using ISA.

7.4.8 IDE Signals

- Series termination resistors should be placed within one inch of the PIIX4E.
- When not using IDE the following primary and secondary IDE signals, they may be left as NO CONNECTS: xDA[2:0], xDCS1#, xDCS3#, xDD[15:8,6:0], xDDACK#, xDIOR#, xDIOW#.

Table 48. IDE Signals

	PIIX4E Pin	Pin Connection
	PDA[2:0]	Connect to IDE connector through 33 Ω series resistors.
	PDCS1#	Connect to IDE connector through 33 Ω series resistor.
	PDCS3#	Connect to IDE connector through 33 Ω series resistor.
	PDD[15:0]	Connect to IDE connector through 33 Ω series resistors. It is recommended that PDD[7] have a 10 KΩ pull-down resistor even if IDE is not used.
	PDDACK#	Connect to IDE connector through 33 Ωseries resistor.
	PDDREQ	Connect to IDE through 33 Ω series resistor. 5.6 KΩ pull-down on the PIIX4E side of the series resistor. When not used, a 5.6 KΩ pull-down is still required.
	PDIOR#	Connect to IDE connector through 33 Ω series resistor.
	PDIOW#	Connect to IDE connector through 33 Ω series resistor.
	PIORDY	Connect to IDE through 47 Ω series resistor. 1 KΩ pull-up to V_{CCISA} on the PIIX4E side of the series resistor. When not used, a 1 KΩ pull-up is still required
	SDA[2:0]	Connect to IDE connector through 33 Ω series resistors.
	SDCS1#	Connect to IDE connector through 33 Ω series resistor.
	SDCS3#	Connect to IDE connector through 33 Ω series resistor.
	SDD[15:0]	Connect to IDE connector through 33 Ω series resistors. It is recommended that SDD[7] have a 10 KΩ pull-down resistor even if IDE is not used.
	SDDACK#	Connect to IDE connector through 33 Ω series resistor.
	SDDREQ	Connect to IDE through 33 Ωseries resistor. 5.6 KΩ pull-down on the PIIX4E side of the series resistor. When not used, a 5.6 KΩ pull-down is still required.
	SDIOR#	Connect to IDE connector through 33 Ω series resistor.
	SDIOW#	Connect to IDE connector through 33 Ω series resistor.
	SIORDY	Connect to IDE through 47 Ω series resistor. 1 KΩ pull-up to V_{CCISA} on the PIIX4E side of the series resistor. When not used, a 1 KΩ pull-up is still required.

7.4.9 USB Signals

- When not using USB, a 10 KΩ pull-up to 3.3 V is required on OC[1:0]# and 15 KΩ pull-downs are required on all USBP signals.
- Refer to the *PIIX4 Universal Serial Bus* design guide and Checklist for USB layout guidelines, available from your Intel field sales representative.

Table 49. USB Signals

	PIIX4E Pin	Pin Connection
	OC[1:0]#	Driven by USB over-current detection voltage divider.
	USBP0+ /USBP0-	47pF cap to Vss with 27 Ω series resistor to USB port. These should be placed as close as possible to the PIIX4E.
	USBP1+ /USBP1-	47pF cap to Vss with 27 Ω series resistor to USB port. These should be placed as close as possible to the PIIX4E.

7.4.10 Power Management Signals

- SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states.
- SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR, and STD suspend states.
- SUSC# is primarily used to control the tertiary power plane. This signal is asserted during STD suspend state.

Table 50. Power Management Signals (Sheet 1 of 2)

	PIIX4E Pin	Pin Connection
	BATLOW# /GPI19	10 KΩ pull-up to 3.3 VSB if BATLOW# is not used. When the Battery Low function is not needed, this pin may be used as a general-purpose input.
	CPU_STP# /GPO17	NO CONNECT, or connect to CK100M with 10 KΩ pull-up to 3.3 VSB.
	EXTSMI#	Connect to LM79. 10 KΩ pull-up to 3.3 VSB.
	LID/GPI10	10 KΩ pull-up to 3.3 VSB if LID is not used.
	PCIREQ[A:D]#	10 KΩ pull-up to 3.3 V. Connect to 82443BX and PCI slots.
	PCI_STP#/GPO18	No connect, or connect to CK100M with 10 KΩ pull-up to 3.3 VSB. When this function is not needed, this pin may be used as a general-purpose output.
	PWRBTN#	From power button circuitry. When not used, add a 10 KΩ pull-up to 3.3 VSB.
	RI#/GPI12	10 KΩ pull-up to 3.3 VSB. Connect to AGP connector AGP_PME# (pin A48). When this function is not needed, this signal may be individually used as a general-purpose input.
	RSMRST#	From ATX connector buffer/delay circuitry. When not using power management (suspend modes), this may be connected to PIIX4E PWROK.
	SMBALERT#/GPI11	10 KΩ pull-up to 3.3 VSB. Connect to MAX1617. When this function is not needed, this pin may be used as a general-purpose input.
	SMBCLK	2.7 KΩ pull-up to 3.3 V. Connect to all devices on SMBus. This value may need to be adjusted based on bus loading.
	SMBDATA	2.7 KΩ pull-up to 3.3 V. Connect to all devices on SMBus. This value may need to be adjusted based on bus loading.
	SUSA#	No connect, or connect to CK100M power down control with 10 K Ω pull-up to 3.3 V.
	SUSB# /GPO15	Controls secondary power plane during STR and STD suspend state. When the power plane control is not needed, this pin may be used as a general-purpose output.
	SUSC#/GPO16	Controls tertiary power plane during STD suspend state. When the power plane control is not needed, this pin may be used as a general-purpose output.
	SUS_STAT1#/GPO20	No Connect or connect to 82443BX for POS implementation. When this function is not needed, this pin may be used as a general-purpose output.
	SUS_STAT2#/GPO21	NO CONNECT. When this function is not needed, this pin may be used as a general-purpose output.
	THRM#/GPI8	10 KΩ pull-up to 3.3 V. Connect to LM75. When this function is not needed, this pin may be used as a general-purpose input.
	ZZ/GPO19	NO CONNECT. When this function is not needed, this pin may be used as a general-purpose output.
	GPI[21:0]	10 KΩ pull-up to 3.3 V if these pins are not used.

Table 50. Power Management Signals (Sheet 2 of 2)

	PIIX4E Pin	Pin Connection
	GPO[30:0]	NO CONNECT if these pins are not used.

7.4.11 Other System and Test Signals

Table 51. Other System and Test Signals

	PIIX4E Pin	Pin Connection
	CONFIG1	10 KΩ pull-up to 3.3 VSB.
	CONFIG2	10 KΩ pull-down to Vss
	PWROK	Connect to 82443BX and power up logic. When not using power management (suspend modes), also connect to PIIX4E RSMRST#.
	SPKR	Connect to speaker circuit. NO CONNECT if not used.
	TEST#	10 KΩ pull-up to 3.3VSB.

7.4.12 Power and Ground Pins

Table 52. Power and Ground Pins

	PIIX4E Pin	Pin Connection
	Vcc	Tie to 3.3 V.
	Vcc(RTC)	Tie to 3.3 V. Connect to battery circuitry. Also referred to as V_{BAT}
	Vcc(SUS)	Tie to 3.3 V Standby plane (Also referred to as 3.3 VSB). The 3.3 VSB should power off only when the system is mechanically off. When power management is not used, tie directly to 3.3 V.
	Vcc(USB)	Tie to 3.3 V.
	V_{REF}	For a 5 V tolerant PCI bus connect to 5 V. It must be powered up before or simultaneous to 3.3 V. It must power down after or simultaneous to 3.3 V. See Section 8.1.1 for example circuit. For non-5 V tolerant PCI (3.3 V only) connect directly to 3.3 V. There are no sequencing requirements.
	Vss	Tie to GND.
	Vss (USB)	Tie to GND.

7.4.13 PIIX4E Decoupling Guidelines

Use the same guidelines as shown in Section 7.3.9, “82443BX Decoupling Guidelines” on page 68.

8.0 Power Sequencing

This section provides a summary of the power sequencing requirements and options of the 440BX AGPset. It provides a detailed description of the PIIX4E Suspend/Resume sequence, signaling protocols, and timings. The recommended usage model for power plane control in a 440BX platform using PIIX4E power management signals is described.

This section does not represent the only way to design a system, but it does provide recommendations for using the 440BX AGPset.

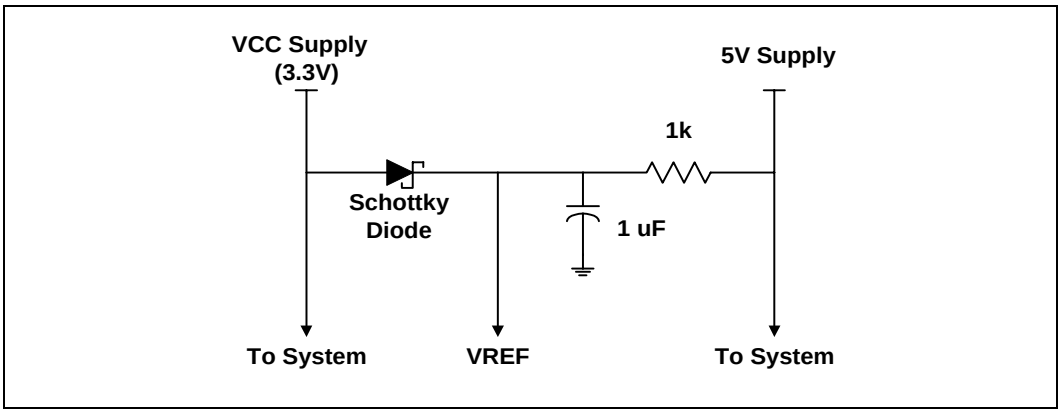
8.1 PIIX4E Power Sequencing

8.1.1 Power Sequencing Requirements

In systems requiring 5 V tolerance, the VREF signal must be tied to 5 V. This signal must power up before or simultaneous to V_{CC}. It must power down after or simultaneous to V_{CC}. In a non 5 V tolerant system (3.3 V only), this signal may be tied directly to V_{CC}. There are then no sequencing requirements. Refer to Figure 34 for an example circuit schematic, which may be used to ensure the proper VREF sequencing.

The PIIX4E V_{CC} and V_{CC}(USB) supplies are separated internally in order to reduce noise on USB signals. They should not be powered up or down independently of one another. They should be connected to the same power plane on the motherboard. There are no other power sequencing requirements for the various V_{CC} power supplies to the PIIX4E.

Figure 34. VREF Supply Schematic



8.1.2 Suspend/Resume and Power Plane Control

The PIIX4E supports three different Suspend modes. The common system usage model for these modes is described here and includes Power On Suspend (POS), Suspend to RAM (STR), and Suspend to Disk (STD). This mode definition allows for other system usage models that use the PIIX4E suspend/resume control signals in other ways. The common system mode names are used throughout this document.

The PIIX4E power management architecture is designed to allow systems to support multiple suspend modes, and to switch between those modes as required. A suspended system may be resumed by a number of different events. The system returns to full operation, and may then continue processing or be placed into another suspend mode. The new mode may be at a lower power mode than the mode from which it resumed.

8.1.2.1 Power On Suspend (POS) System Model

All devices are powered up except for the clock synthesizer. The Host and PCI clocks are inactive, and the PIIX4E provides control signals and the 32 KHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer. The only power consumed in the system while it is in POS mode is due to DRAM refresh and leakage current of the powered devices.

When the system resumes from POS mode, the PIIX4E may resume without resetting the system, may reset the processor only, or may reset the entire system. When no reset is performed, the PIIX4E only needs to wait for the clock synthesizer and processor PLLs to lock before the system is resumed. This takes typically 20 ms.

8.1.2.2 Suspend to RAM (STR)

Power is removed from most of the system components during STR, except the DRAM. Power is supplied to the host bridge (for DRAM Suspend Refresh) and the PIIX4E's RTC and Suspend Well logic. The PIIX4E provides control signals and a 32 KHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer and other power planes.

The PIIX4E resets the system on resume from STR.

8.1.2.3 Suspend to Disk (STD) and Soft Off (SOff)

Power is removed from most of the system components during STD. Power is maintained to the RTC and Suspend Well logic in the PIIX4E.

The PIIX4E resets the system on resume from STD.

The STD state is also called the Soft Off (SOff) state. The difference depends on whether the system state is restored by software to a pre-suspend condition or the system is rebooted.

8.1.2.4 Mechanical Off (MOff)

This is not a suspend state. This is a condition where all power except the RTC battery has been removed from the system. It is typically controlled by a mechanical switch that turns off AC power to a power supply. It could be used as a condition in which an embedded system's main battery has been removed.

The PIIX4E controls the system entering the various suspend states through the suspend control signals listed in Table 53. Upon initiation of suspend, the PIIX4E asserts the SUS_STAT[1-2]#, SUSA#, SUSB#, and SUSC# signals in a well defined sequence to switch the system into the desired power state. The SUSA#, SUSB#, and SUSC# signals may be used to control various power planes in the system. The SUS_STAT1# signal is a status signal that indicates to the host bridge when to enter or exit a suspend state, or when to enter or exit a stop clock state (when the system is still running). This is typically used to place the DRAM controller into a Suspend Refresh mode of operation. The SUS_STAT2# signal is a status signal that may be used to indicate to other system devices when to enter or exit a suspend state (like the graphics and Cardbus controllers). See "System Suspend and Resume Control Signaling" on page 84 for sequencing details. Note that these signals are associated with a particular type of suspend mode and power plane for descriptive purposes here. The system designer is free to use these signals to control any type of function desired.

The system is placed into a suspend mode by programming the Power Management Control register. The Suspend Type is first programmed and then the Suspend Enable bit is set. This causes the PIIX4E to automatically sequence into the programmed suspend mode.

Table 53. Power State Decode

Power State	RSMRST#	SUS_STAT1#	SUS_STAT2#	SUSA#	SUSB#	SUSC#
On	1	x†	1	1	1	1
POS	1	0	0	0	1	1
STR	1	0	0	0	0	1
STD/SOFF	1	0	0	0	0	0
Mechanical Off	0	0	0	0	0	0

† SUS_STAT1# is also used when the system is running. It indicates to the Host-to-PCI bridge when to switch between the normal and suspend refresh mode for DRAM Stop Clock support. In the Stop Clock condition, HCLK is stopped and the Host-to-PCI bridge must run DRAM refresh from the internal oscillator.

8.1.3 System Resume

The PIIX4E may be resumed from either a Suspend or Soft Off state. Depending on the suspend state that the system is in, different features may be enabled to resume the system. There are two classes of resume events, those whose logic resides in the PIIX4E main power well and those whose logic resides in the PIIX4E suspend well. Those in the suspend well may resume the system from any Suspend or Soft Off state. Those in the main power well may only resume the system from a Power On Suspend state. Table 54 lists the suspend states for which a particular resume event may be enabled.

Upon detection of an enabled resume event, the PIIX4E sets appropriate status signals and automatically transitions its suspend control signals to bring the system into a 'full on' condition. The sequencing is shown in "System Suspend and Resume Control Signaling" on page 84.

Table 54. Resume Events Supported In Different Power States

Resume Event	Suspend States			
	POS	STR	STD/SOff	MOff
RTC Alarm (IRQ8) †	x	x	x	
SMBus Resume Event (Slave Port Match)	x	x	x	
Serial A Ring (RI)	x	x	x	
Power Button (PWRBTN#)	x	x	x	
EXTSMI (EXTSMI#)	x	x	x	
LID (LID)	x	x	x	
GPI 1	x	x	x	
GSTBY Timer Expiration	x	x	x	
Interrupt (IRQ 1,3-15)	x			
USB	x			

† RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#,RI#) for the resume functionality.

8.1.3.1 System Resume Events

Table 55 indicates the various resume events and their corresponding programming models.

Table 55. Resume Event Programming Model

System Resume Event	Programming Model
PWRBTN# Asserted	[PWRBTN_EN]
LID Asserted - Polarity Select	[LID_EN] [LID_POL]
GPI[1] Asserted	[GPI_EN]
EXTSMI# Asserted	[EXTSMI_EN]
SMBus Events:	[ALERT_EN] [SLV_EN] [SHDW1_EN] [SHDW2_EN]
Global Standby Timer Expiration:	[GSTBY_EN]
Ring Indicate Assertion (RI#)	[RI_EN]
RTC Alarm (IRQ8)†	[RTC_EN]
USB Resume Signaling: (POS Only)	[USB_EN]
IRQ[1,3-7,9-15]: (POS Only)	[IRQ_RSM_EN]

† RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#,RI#) for the resume functionality.

8.1.3.2 Global Standby Timer Resume

The Global Standby Timer is used to monitor system activity during normal operation and may be reloaded by system activity events. Upon expiration, it generates an SMI#. When the system is placed in a Suspend Mode, the Global Standby Timer may be used to generate a resume event. The Global Standby Timer may enable two different timer resolutions for wake-up times from approximately 30 seconds to 8.5 hours. This may allow the system to transition into a lower power suspend state.

See the System Management Section of the *Intel® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) Datasheet* (order number 290562) for additional information about the Global Standby Timer.

8.1.4 System Suspend and Resume Control Signaling

The PIIX4E automatically controls the signals required to transition the system between the various power states. It provides control for Host and PCI clocks, main memory and video memory refresh, system power plane control, and system reset. Table 56 and Table 57 indicate the common usage model for power plane control using the SUS[C:A]# signals. The PIIX4E Resume well should always be powered by a trickle supply (main battery or backup battery in an embedded system).

Table 56. Power Plane Control

SUSA# (POS)	SUSB# (STR)	SUSC# (STD)
Clock synthesizer Video display[1]	Processor (Low Power GTL+ supplies) PIIX4E Core Other system devices[2]	82443BX Host Bridge/Controller DRAM Graphics Controller

NOTES:
1. The video display (flat panel or CRT) may optionally be powered off in POS. This could be accomplished by using the PIIX4E's SUSA# or SUS_STAT2# signals to assert the video controller's STANDBY signal.
2. Devices may include mass storage, audio, or other devices that will not generate system resume events.

Table 57. Power Plane Control Using SUS[C:A]# Signals

Power Plane	Suspend Mode (Suspend Mode Signals Asserted by the PIIX4E)			
	Full On (None)	POS (SUSA#, SUS_STAT[2:1]#)	STR (SUS[B:A]# SUS_STAT[2:1]#)	STD (SUS[C:A]# SUS_STAT[2:1]#)
Clock Synthesizer	On	Off	Off	Off
Video Display	On	On/Off[1]	Off	Off
CPU	On	On	Off	Off
PIIX4E Core	On	On	Off	Off
Other Devices[2]	On	On	Off	Off
82443BX	On	On	On	Off
DRAM	On	On	On	Off
Graphics Controller	On	On	On	Off
PIIX4E Resume	On	On	On	On
PIIX4E RTC	On	On	On	On

NOTES:
1. The video display (flat panel or CRT) may optionally be powered off in POS. This could be accomplished by using the PIIX4E's SUSA# or SUS_STAT2# signals to assert the video controller's STANDBY signal.
2. Devices may include mass storage, audio, or other devices that will not generate system resume events.

8.1.4.1 Power Well and Reset Signal Timings

Figure 35 shows the system timings for changing the power states of a system using the POS/STR/STD models.

8.1.4.2 PIIX4E Power Well Timings

Figure 35 describes the relative transitions for PIIX4E power supplies. Table 58 indicates the PIIX4E power well timing tolerances.

Figure 35. PIIX4E Power Well Timings

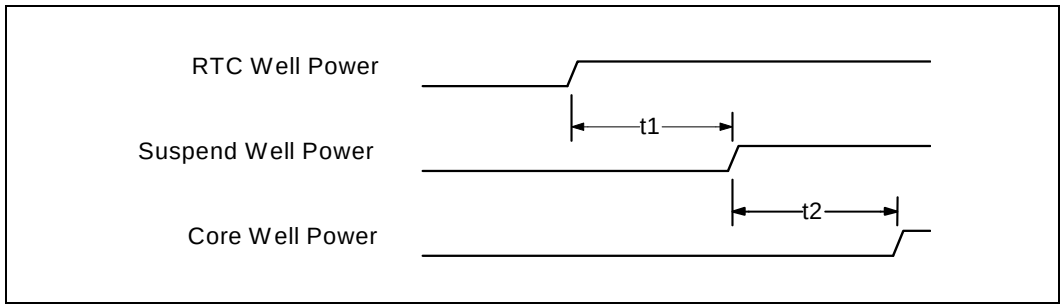


Table 58. PIIX4E Power Well Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t1	RTC Well Power to Suspend Well Power	0		ns	
t2	Suspend Well Power to Core Well Power	0		ns	

8.1.4.3 RSMRST# and PWROK Timing

Figure 36 describes the required timings for PIIX4E power level active status signals. Table 59 indicates the RSMRST# and PWROK timing tolerances.

Figure 36. RSMRST# and PWROK Timings

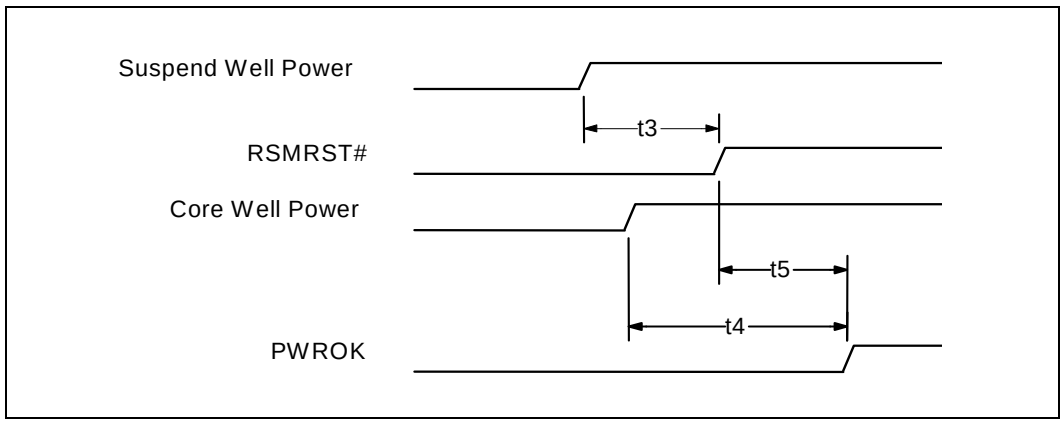


Table 59. RSMRST# and PWROK Timing Tolerance

Sym	Parameter	Min	Max	Unit	Notes
t3	Suspend Well Power to RSMRST# Inactive	1		ms	
t4	Core Well Power to PWROK Active	1		ms	
t5	RSMRST# Inactive to PWROK Active	0		ns	

8.1.4.4 Suspend Well Power and RSMRST# Activated Signals

Figure 37 shows the timing relationships for the PIIX4E power management signals that are powered from the Suspend Well Power signal. These timings hold independent of the condition of Core Well Power or the PWROK signal. Table 60 indicates the Suspend Well Power and RSMRST# timing tolerances.

Figure 37. Suspend Well Power and RSMRST# Activated Signals

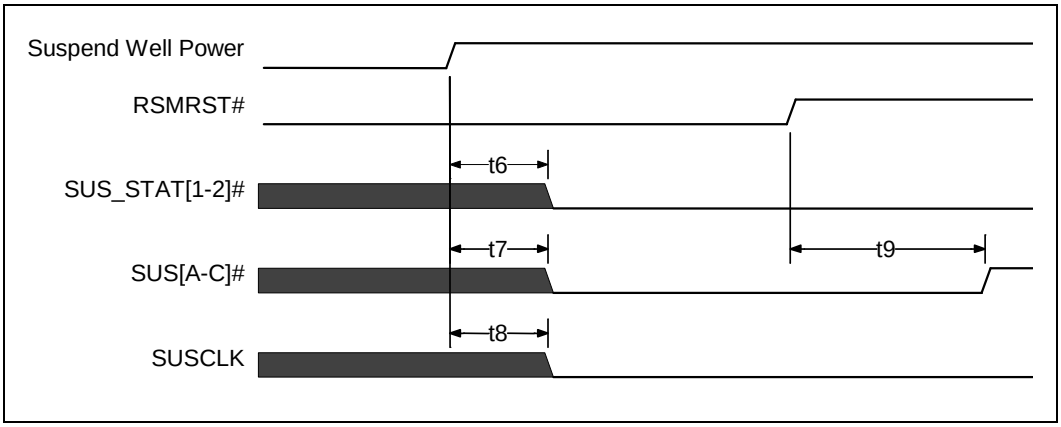


Table 60. Suspend Well Power and RSMRST# Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t6	Resume Well Power and RSMRST# Active to SUS_STAT[1:2]# Active		1	RTC	†
t7	Resume Well Power and RSMRST# Active to SUS [A:C]# Active		1	RTC	†
t8	Resume Well Power and RSMRST# Active to SUSCLK Low		1	RTC	†
t9	RSMRST# Inactive to SUS[A:C]# Inactive	1	2	RTC	†

† These signals are controlled off an internal RTC clock. One RTC unit is approximately 32 µs.

8.1.4.5 PCI Clock Control Timings

This section describes the timing requirements for the control of the system PCICLK. The system PCICLK timing shown in Figure 38 must be followed exactly for proper operation of the PC/PCI DMA or Serial IRQ logic. When the PC/PCI DMA and Serial IRQs are not used in the system, the system PCICLK stop timings must meet the system developer's requirements.

Figure 38. PCI Clock Stop Timing

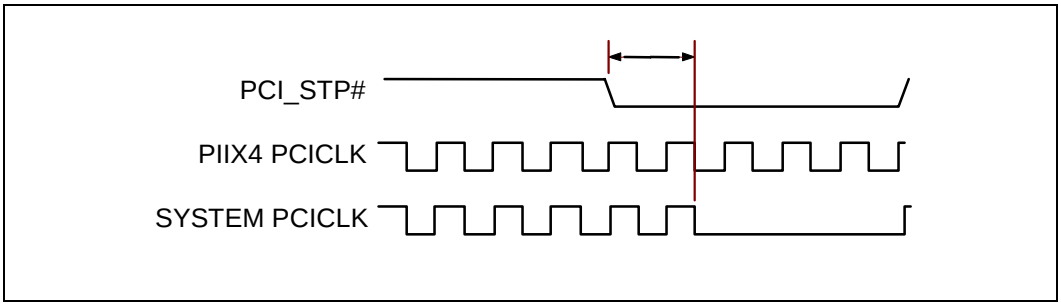
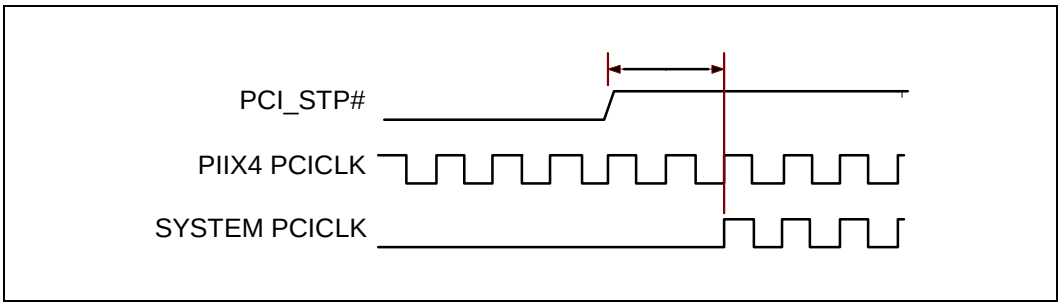


Figure 39 describes the timing requirements for the control of the system PCICLK. The system PCICLK timings shown in Figure 39 must be followed exactly for proper operation of PC/PCI DMA or Serial IRQ logic. When PC/PCI DMA and Serial IRQs are not used in the system, the system PCICLK stop timings must meet the system developer's requirements.

Figure 39. PCI Clock Start Timing



8.1.4.6 Core Well Power and PWROK Activated Signals (RSMRST# Inactive Before Core Well Power Applied)

Figure 40 shows the timing relations for Power Management signals powered from the PIIX4E Main Core well. The Suspend Well Power active status signals (RSMRST#) transitions before the application of core well power to the PIIX4E. This figure corresponds to the usage model for PIIX4E power management. Table 61 indicates the Core Well Power and PWROK timing tolerances.

Figure 40. Core Well Power and PWROK Activated Signals (RSMRST# Inactive before Core Well Power Applied)

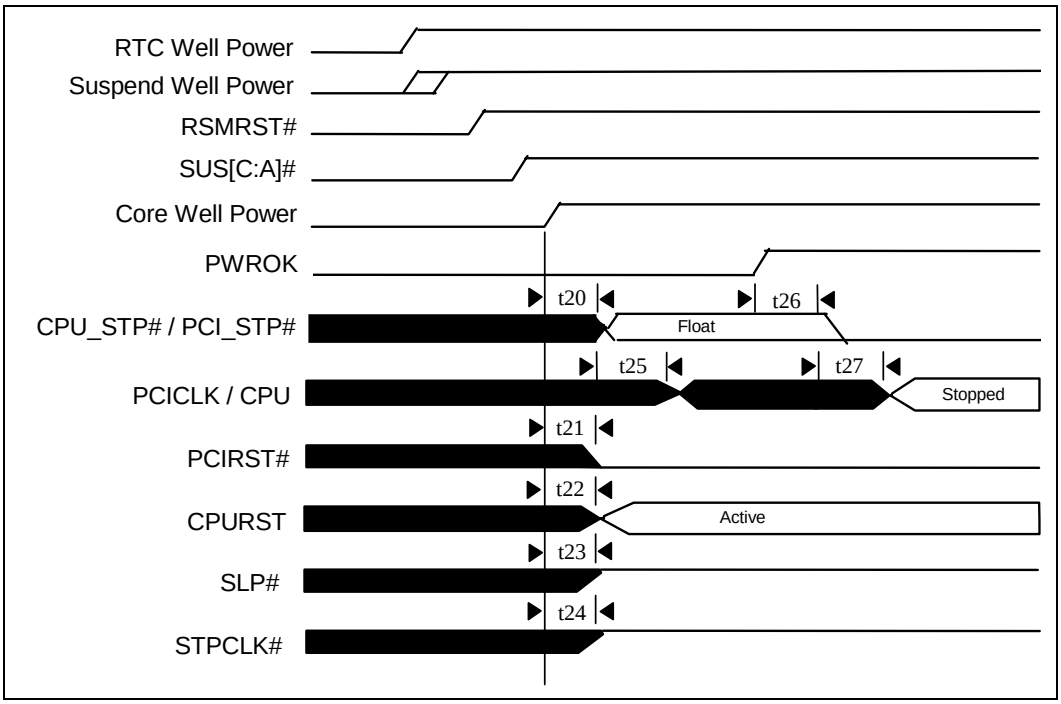


Table 61. Core Well Power and PWROK Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t20	Core Well Power and PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t21	Core Well Power and PWROK Inactive to PCIRST# Active		1	RTC	1
t22	Core Well Power and PWROK Inactive to CPURST Active		1	RTC	1
t23	Core Well Power and PWROK Inactive to SLP# Active		1	RTC	1
t24	Core Well Power and PWROK Inactive to STPCLK# Active		1	RTC	1
t25	CPU_STP# and PCI_STP# Float to Clocks Running				2
t26	PWROK Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t27	CPU_STP# and PCI_STP# Active to Clocks Stopped				2

NOTES:
1. These signals are controlled off an internal RTC clock. One RTC unit is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. As a minimum, the clocks must be available and stable after time t29 shown in Figure 42.

8.1.4.7 Core Well Power and PWROK Activated Signals (Core Well Power Applied Before RSMRST# Inactive)

Figure 41 shows the timing relations for Power Management signals powered from the PIIX4E Core well. Here the power active status signals (RSMRST# and PWROK) transition after the application of all power to the PIIX4E. This is an example of an implementation in which the Core Well power plane is not controlled by the SUSB# signal. It may be applied to situations where two or more of the PIIX4E power planes are connected together. It also shows timings when RSMRST# and PWROK are connected together.

Figure 41. Core Well Power and PWROK Activated Signals (Core Well Power Applied before RSMRST# Inactive)

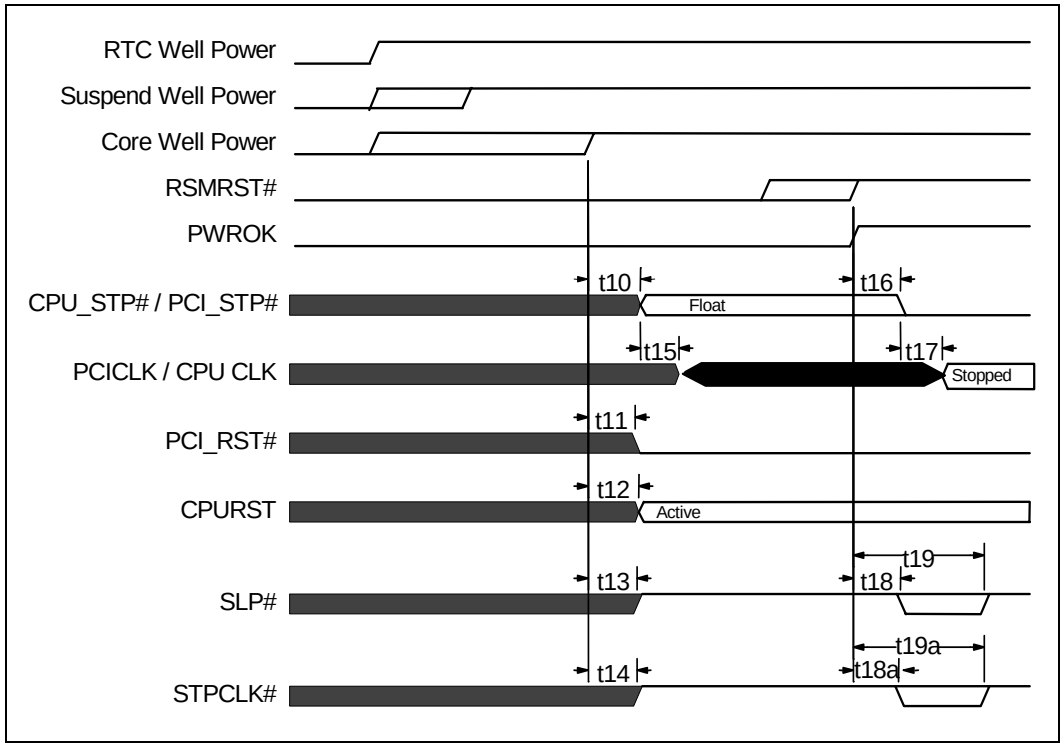


Table 62. Core Well Power and PWROK Timing

Sym	Parameter	Min	Max	Unit	Notes
t10	Core Well Power and PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t11	Core Well Power and PWROK Inactive to PCIRST# Active		1	RTC	1
t12	Core Well Power and PWROK Inactive to CPURST Active		1	RTC	1
t13	Core Well Power and PWROK Inactive to SLP# Inactive		1	RTC	1
t14	Core Well Power and PWROK Inactive to STPCLK# Inactive		1	RTC	1
t15	CPU_STP# and PCI_STP# Float to Clocks Running				2
t16	PWROK Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t17	CPU_STP# and PCI_STP# Active to Clocks Stopped				2
t18	PWROK Active to SLP# Active	0		ns	3
t18a	PWROK Active to STPCLK# Active	0		ns	1
t19	PWROK Active to SLP# Inactive	1	2	RTC	1, 3
t19a	PWROK Active to STPCLK# Inactive	1	2	RTC	1, 3

NOTES:
1. These signals are controlled off an internal RTC clock. One RTC unit is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. As a minimum, the clocks must be available and stable after time t29 shown in Figure 42.
3. These timings depend on the relative timings between RSMRST# and PWROK. When RSMRST# goes inactive two RTC periods before PWROK active, SLP# and STPCLK# will remain inactive. When RSMRST# goes inactive less than two RTC periods before PWROK active, an active pulse will be seen on SLP# and STPCLK#.

8.1.5 Power Management State Transition Timings

8.1.5.1 Mechanical Off to On

Figure 42 shows the transition from a Mechanical Off condition to the On condition. Table 63 describes the mechanical Off to On timing tolerances.

Figure 42. Mechanical Off to On

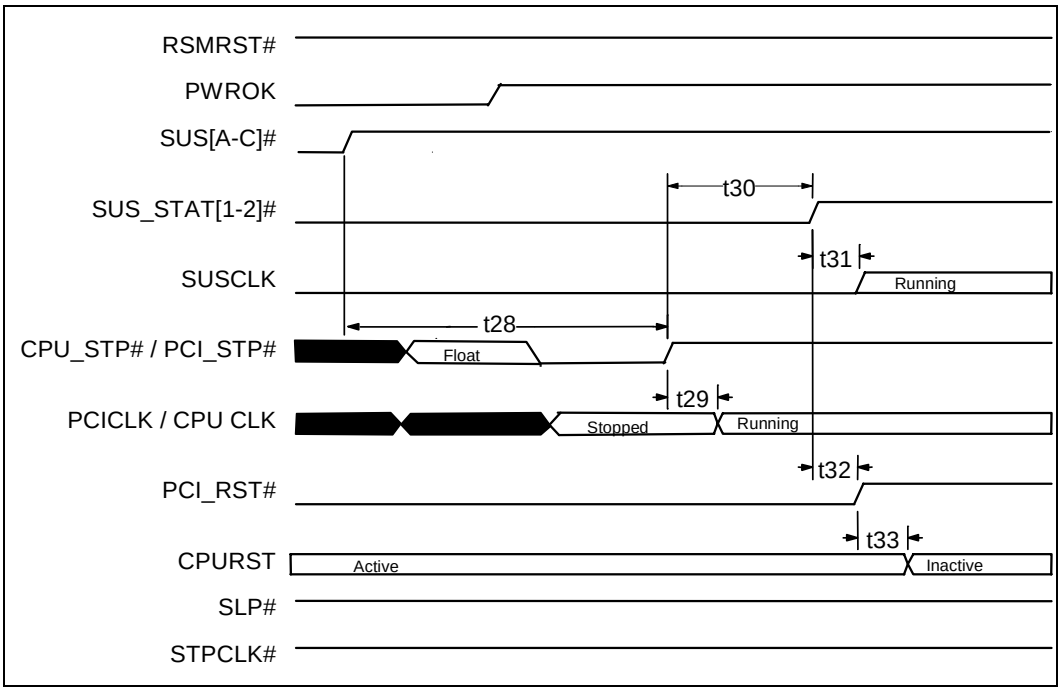


Table 63. Mechanical Off to On Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t28	SUS[A:C]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	1
t29	CPU_STP# and PCI_STP# Inactive to Clocks Running		2	PCICLK	2
t30	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t31	SUS_STAT[1:2]# Inactive to SUSCLK Running		1	RTC	3
t32	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive		1	RTC	3
t33	PCI_RST# Inactive to CPURST Inactive		1	RTC	3

NOTES:
1. This transition requires a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. When PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition occurs a minimum of one RTC period from PWROK active.
2. See Figure 38 and Figure 39 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.
3. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32 µs.

8.1.5.2 On to POS

Figure 43 describes the signal transitions from the On state to the Power On Suspend state. Table 64 indicates the On to POS timing tolerances.

Figure 43. On to POS

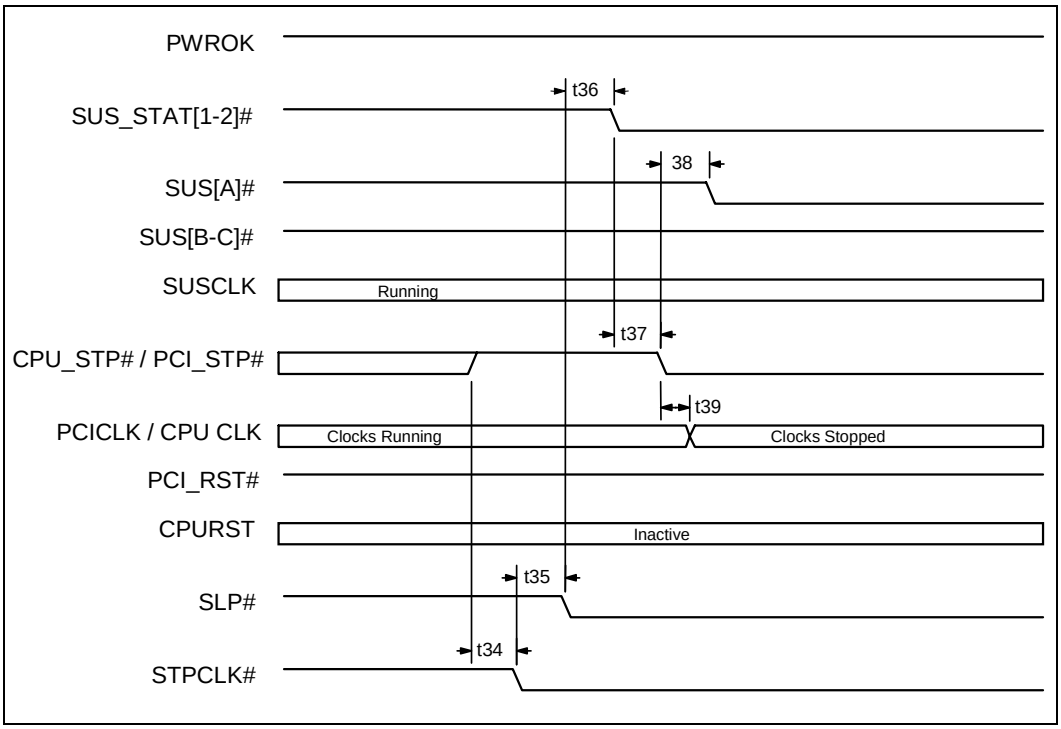


Table 64. On to POS Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t34	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t35	STPCLK# Active to SLP# Active	1		RTC	1, 3
t36	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t37	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active	1		RTC	1
t38	CPU_STP# and PCI_STP# Active to SUS[A]# Active		1	RTC	1
t39	CPU_STP# and PCI_STP# Active to Clocks Stopped (if applicable)		2	PCICLK	4, 5

NOTES:
1. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32 µs.
2. CPU_STP# and PCI_STP# will only be active when the system is under clock control.
3. This transition waits for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine whether CPU_STP# and PCI_STP# signals are used to control system clocks.
5. See Figure 38 and Figure 39 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

8.1.5.3 POS to On (with Processor and PCI Reset)

Figure 44 describes the system transition from Power On Suspend to On with a full system reset. Table 65 indicates the POS to On timing tolerances.

Figure 44. POS to On (with Processor and PCI Reset)

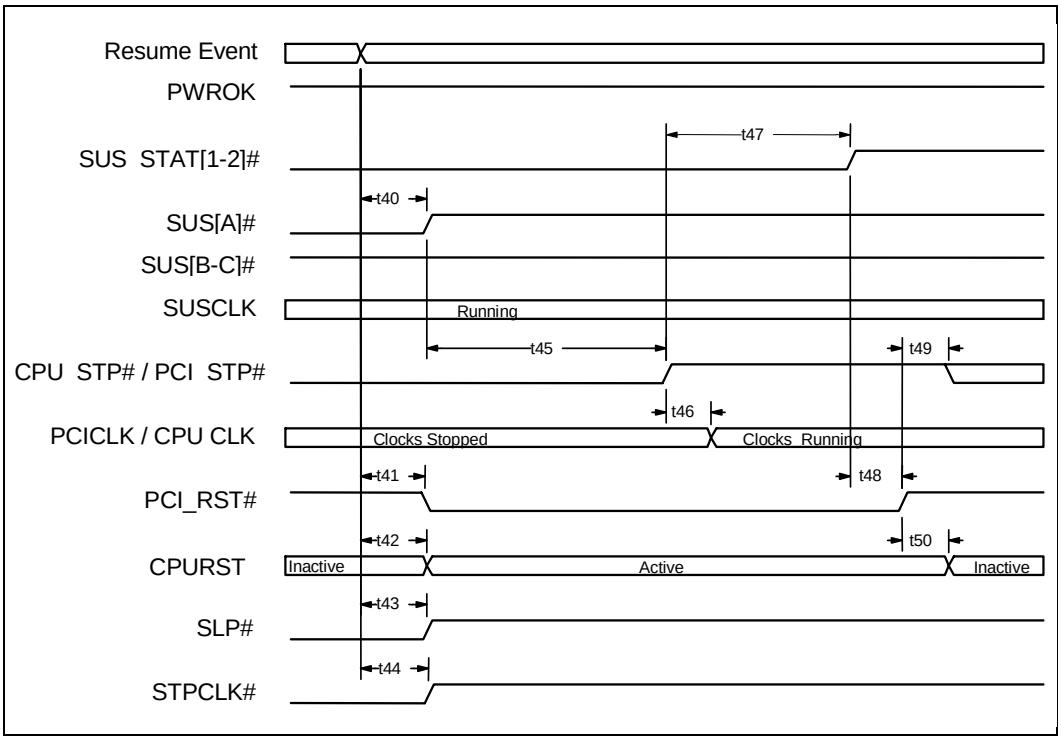


Table 65. POS to On Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t40	Resume Event to SUS[A]# Inactive	1		RTC	1
t41	Resume Event to PCI_RST# Active	1		RTC	1
t42	Resume Event to CPURST Active	1		RTC	1
t43	Resume Event to SLP# Inactive	1		RTC	1
t44	Resume Event to STPCLK# Inactive	1		RTC	1
t45	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t46	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3
t47	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t48	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive		1	RTC	1
t49	PCI_RST# Inactive to PCI_STP# and CPU_STP# allowed to change		1	RTC	1
t50	PCI_RST# Inactive to CPURST Inactive		1	RTC	1

NOTES:
1. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32 µs.
2. This transition requires a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. When PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Figure 38 and Figure 39 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

8.1.5.4 POS to On (with Processor Reset)

Figure 45 describes the system transition from Power On Suspend (POS) to On with only a processor reset. Table 66 indicates the POS to On (with processor reset) timing tolerances.

Figure 45. POS to On (with Processor Reset)

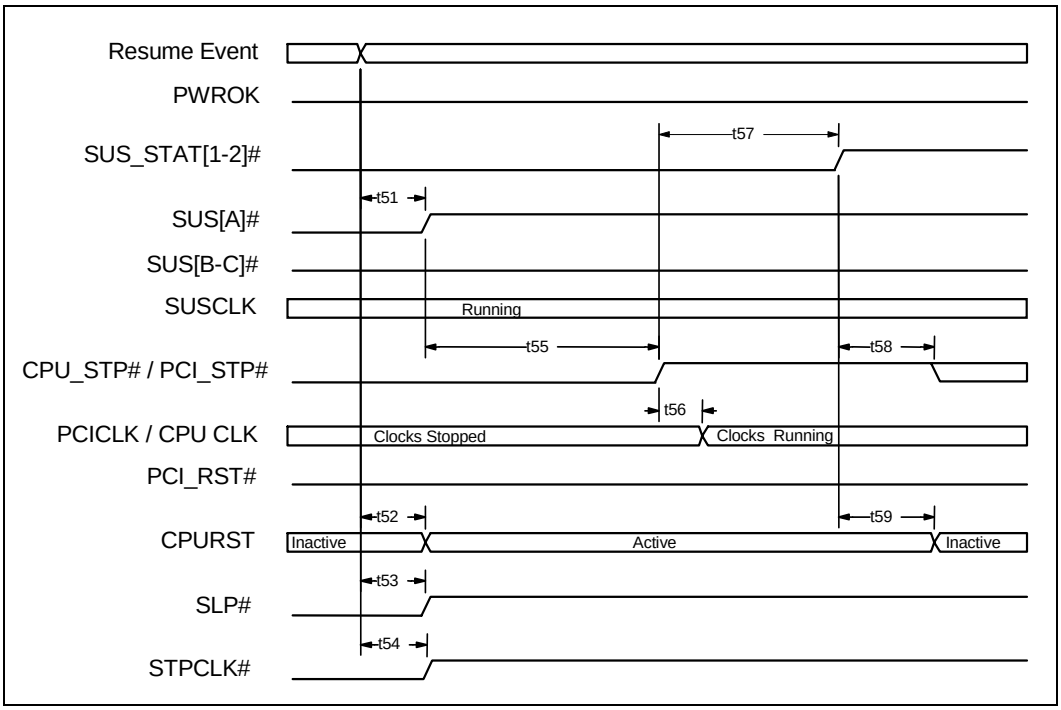


Table 66. POS to On (with Processor Reset) Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t51	Resume Event to SUSA# Inactive	1		RTC	1
t52	Resume Event to CPURST Active	1		RTC	1
t53	Resume Event to SLP# Inactive	1		RTC	1
t54	Resume Event to STPCLK# Inactive	1		RTC	1
t55	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t56	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3
t57	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t58	SUS_STAT[1:2]# Inactive to PCI_STP# and CPU_STP# allowed to change		2	RTC	1
t59	SUS_STAT[1:2]# Inactive to CPURST Inactive		2	RTC	1

NOTES:
1. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32 µs.
2. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. When PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Figure 38 and Figure 39 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

8.1.5.5 POS to On (No Reset)

Figure 46 describes the system transition from Power On Suspend to On with no resets performed. Table 67 indicates the POS to On (no reset) timing tolerances.

Figure 46. POS to On (No Reset)

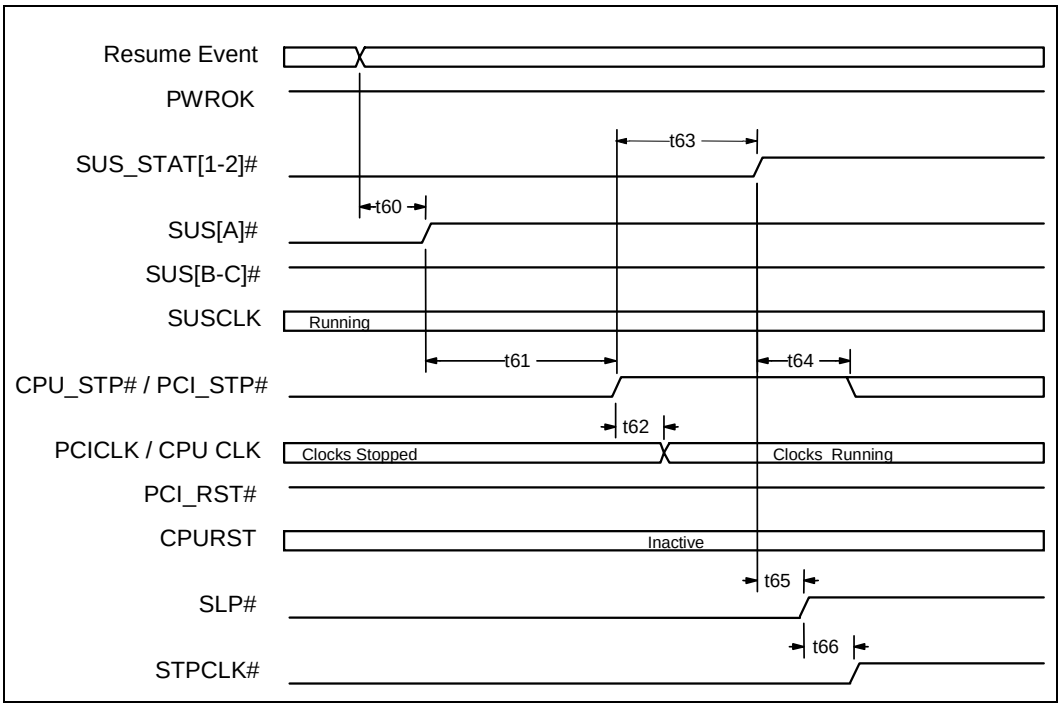


Table 67. POS to On (No Reset) Timing

Sym	Parameter	Min	Max	Unit	Notes
t60	Resume Event to SUS[A]# Inactive	1		RTC	1
t61	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t62	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3
t63	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t64	SUS_STAT[1:2]# Inactive to PCI_STP# and CPU_STP# allowed to change		2	RTC	1
t65	SUS_STAT[1:2]# Inactive to SLP# Inactive		1	RTC	1
t66	SLP# Inactive to STPCLK# Inactive		1	RTC	1

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. When PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Figure 38 and Figure 39 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

8.1.5.6 On to STR

Figure 47 describes the signal transitions from On state to Suspend to RAM state. Table 68 indicates the On to STR timing tolerances.

Figure 47. On to STR

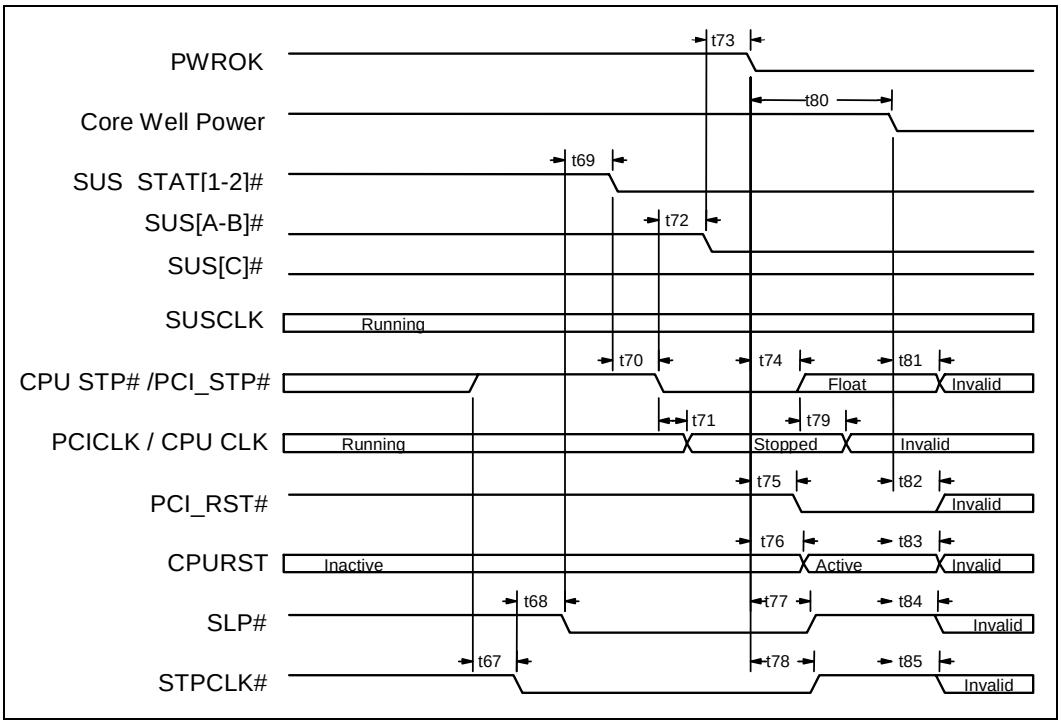


Table 68. On to STR Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t67	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t68	STPCLK# Active to SLP# Active	1		RTC	1, 3
t69	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t70	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t71	CPU_STP# and PCI_STP# Active to CLOCKS Stopped		2	PCICLK	4, 5
t72	CPU_STP# and PCI_STP# Inactive to SUS[A:B]# Active		1	RTC	1
t73	SUS[A:B]# Active to PWROK Inactive	0		ns	6
t74	PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t75	PWROK Inactive to PCI_RST# Active		1	RTC	1
t76	PWROK Inactive to CPURST Active		1	RTC	1
t77	PWROK Inactive to SLP# Inactive		1	RTC	1
t78	PWROK Inactive to STPCLK# Inactive		1	RTC	1
t79	CPU_STP# and PCI_STP# Float to Clocks Invalid	0		ns	7
t80	PWROK Inactive to Core Well Power Removed	0		ns	
t81	Core Well Power Removed to PCI_STP# and CPU_STP# Invalid	0		ns	
t82	Core Well Power Removed to PCIRST# Invalid	0		ns	
t83	Core Well Power Removed to CPURST Invalid	0		ns	
t84	Core Well Power Removed to SLP# Invalid	0		ns	
t85	Core Well Power Removed to STPCLK# Invalid	0		ns	

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. CPU_STP# and PCI_STP# will only be active if the system is under clock control.
3. This transition will also wait for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine if CPU_STP# and PCI_STP# signals are used to control system clocks.
5. See Figure 38 and Figure 39 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.
6. It is up to the system vendor to determine if SUS[A:B]# signals are used to control system power planes. When power remains applied to system board and PWROK stays active during STR, the PIIX4E signals will remain in the states shown after t73.
7. Clocks may or may not be running depending on the condition of the Power Supply voltages.

8.1.5.7 STR to On

Figure 48 describes the system transition from Suspend To RAM to On with a full system reset. Table 56 indicates the STR to On timing tolerances.

Figure 48. STR to On

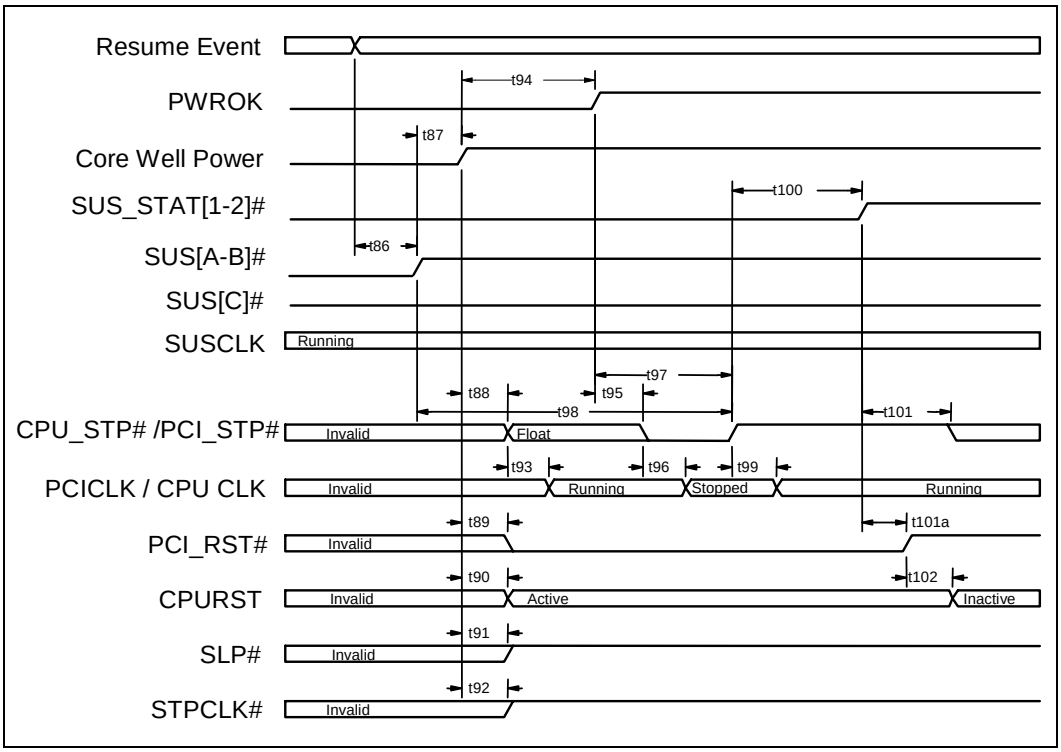


Table 69. STR to On Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t86	Resume Event to SUS[A:B]# Inactive	1		RTC	1
t87	SUS[A:B]# Inactive to Core Well Power Applied	0		ns	
t88	Core Well Power Applied to PCI_STP# and CPU_STP# Float	0		ns	
t89	Core Well Power Applied to PCI_RST# Active	0		ns	
t90	Core Well Power Applied to CPURST Active	0		ns	
t91	Core Well Power Applied to SLP# Inactive	0		ns	
t92	Core Well Power Applied to STPCLK# Inactive	0		ns	
t93	PCI_STP# and CPU_STP# Float to Clocks Running				2
t94	Core Well Power Applied to PWROK Active	1		ms	
t95	PWROK Active to CPU_STP# and PCI_STP# Active	0		ns	
t96	PCI_STP# and CPU_STP# Active to Clocks Stopped		2	PCICLK	3
t97	PWROK Active to CPU_STP# and PCI_STP# Inactive	1		RTC	1
t98	SUS[A-B]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	
t99	CPU_STP# and PCI_STP# Inactive to Clocks Running		2	PCICLK	3
t100	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1-2]# Inactive	1		ms	
t101	SUS_STAT[1-2]# Inactive to CPU_STP# and PCI_STP# allowed to change	2		RTC	1
t101a	SUS_STAT[1-2]# Inactive to PCI_RST# Inactive	1		RTC	1
t102	PCI_RST# Inactive to CPURST Inactive	1		RTC	1

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks meet any other system specifications upon power up. At a minimum, the clocks must be available and stable after time t99.
3. See Figure 38 and Figure 39 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

8.1.5.8 On to STD/SOff

Figure 49 describes the signal transitions from the On state to the Suspend to Disk/Soft Off state. Table 70 indicates the On to STD/SOff timing tolerances.

Figure 49. On to STD/SOff

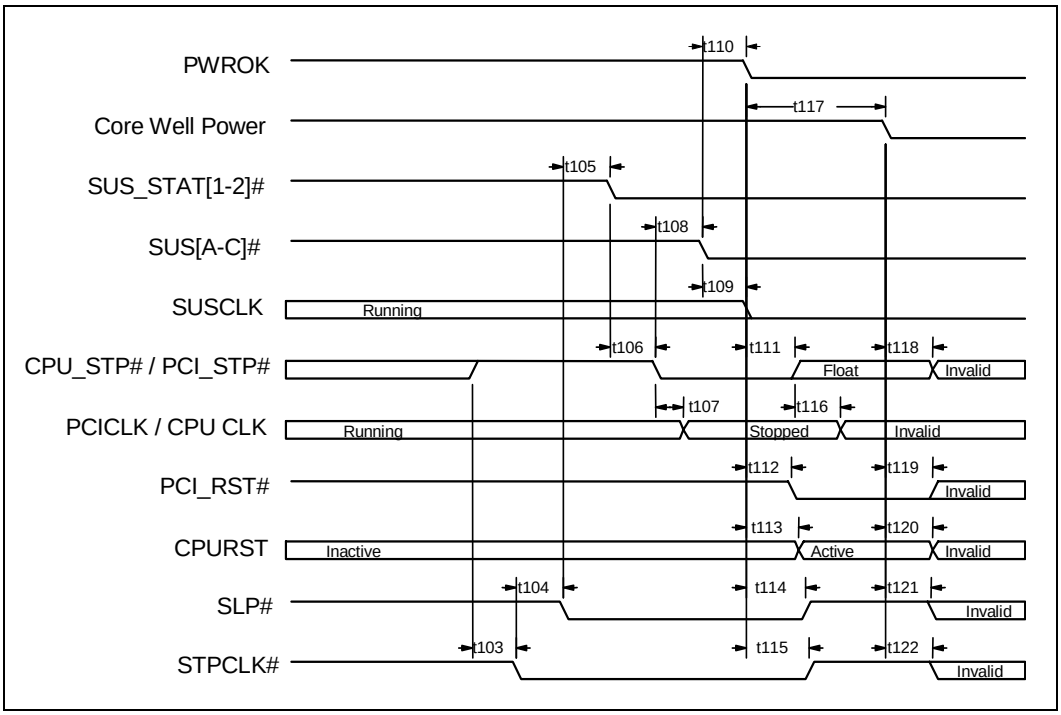


Table 70. On to STD/SOff Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t103	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t104	STPCLK# Active to SLP# Active	1		RTC	1, 3
t105	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t106	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t107	CPU_STP# and PCI_STP# Inactive to CLOCKS Stopped		2	PCICLK	1, 4, 5
t108	CPU_STP# and PCI_STP# Inactive to SUS[A:C]# Active		1	RTC	1
t109	SUS[A:C]# Active to SUSCLK Low		1	RTC	1
t110	SUS[A:C]# Active to PWROK Inactive	0		ns	6
t111	PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t112	PWROK Inactive to PCI_RST# Active		1	RTC	1
t113	PWROK Inactive to CPURST Active		1	RTC	1
t114	PWROK Inactive to SLP# Inactive		1	RTC	1
t115	PWROK Inactive to STPCLK# Inactive		1	RTC	1
t116	CPU_STP# and PCI_STP# Float to Clocks Invalid	0		ns	1
t117	PWROK Inactive to Core Well Power Removed	0		ns	
t118	Core Well Power Removed to PCI_STP# and CPU_STP# Invalid	0		ns	
t119	Core Well Power Removed to PCIRST# Invalid	0		ns	
t120	Core Well Power Removed to CPURST Invalid	0		ns	
t121	Core Well Power Removed to SLP# Invalid	0		ns	
t122	Core Well Power Removed to STPCLK# Invalid	0		ns	

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. CPU_STP# and PCI_STP# will only be active if the system is under clock control.
3. This transition will also wait for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine if CPU_STP# and PCI_STP# signals are used to control system clocks.
5. See Figure 38 and Figure 39 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.
6. It is up to the system vendor to determine if SUS[A:C]# signals are used to control system power planes. When the power remains applied to the system board and the PWROK stays active during STD, the PIIX4E signals will remain in the states shown after t110.

8.1.5.9 STD/SOff to On

Figure 50 describes the system transition from Suspend To Disk/Soft Off to On with a full system reset. Table 71 indicates the STD/SOff to On timing tolerances.

Figure 50. STD/SOff to On

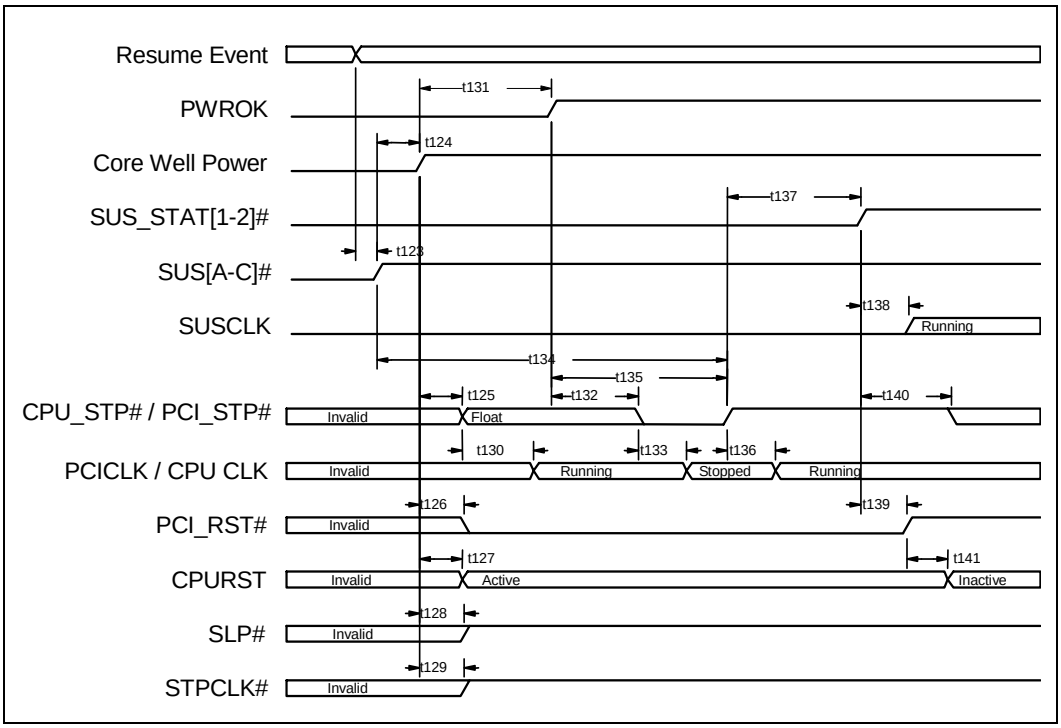


Table 71. STD/SOff to On Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t123	Resume Event to SUS[A:C]# Inactive	1		RTC	1
t124	SUS[A-C]# Inactive to Core Well Power Applied	0		ns	
t125	Core Well Power Applied to PCI_STP# and CPU_STP# Float	0		ns	
t126	Core Well Power Applied to PCI_RST# Active	0		ns	
t127	Core Well Power Applied to CPURST Active	0		ns	
t128	Core Well Power Applied to SLP# Inactive	0		ns	
t129	Core Well Power Applied to STPCLK# Inactive	0		ns	
t130	PCI_STP# and CPU_STP# Float to Clocks Running				2
t131	Core Well Power Applied to PWROK Active	1		ms	
t132	PWROK Active to CPU_STP# and PCI_STP# Active	0		ns	
t133	PCI_STP# and CPU_STP# Active to Clocks Stopped		2	PCICLK	3
t134	SUS[A-C]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	
t135	PWROK Active to CPU_STP# and PCI_STP# Inactive	1		RTC	1
t136	PCI_STP# and CPU_STP# Active to Clocks Running	1	2	PCICLK	3
t137	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t138	SUS_STAT[1:2]# Inactive to SUSCLK Running		1	RTC	1
t139	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive	1		RTC	1
t140	SUS_STAT[1:2]# Inactive to CPU_STP# and PCI_STP# allowed to change	2		RTC	1
t141	PCI_RST# Inactive to CPURST Inactive	1		RTC	1

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. At a minimum, the clocks must be available and stable after time t136.
3. See Figure 38 and Figure 39 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

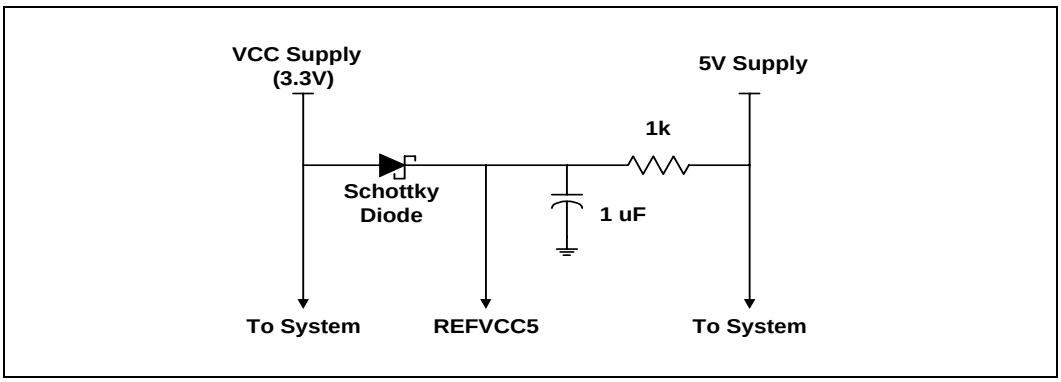
8.2 82443BX Host Bridge/Controller Power Sequencing

8.2.1 Power Sequencing Requirements

In systems requiring 5 V tolerance, the REF5V signal must be tied to 5 V. This signal must power up before or simultaneous to V_{CC}. It must power down after or simultaneous to V_{CC}. In a non-5 V tolerant system (3.3 V only), this signal may be tied directly to V_{CC}. There are then no sequencing requirements. Refer to Figure 51 for an example circuit schematic that may be used to ensure the proper REF5V sequencing. This is the same circuit that is recommended for the PIIX4E VREF supply. However, different power planes may supply the PIIX4E core and the 82443BX Host Bridge/Controller (the PIIX4E core may be powered down during STR). In this case a separate circuit must be used for each of the two devices.

V_{CC} must power up before or simultaneous to the AGP supplies (VCC_AGP and AGP_REF) and Low Power GTL+ supplies (VTT and GTL_REF). V_{CC} must power down after or simultaneous to the AGP and Low Power GTL+ supplies. The AGP and Low Power GTL+ supplies must not be powered up while V_{CC} is powered down. There are no other power sequencing requirements for the 82443BX Host Bridge/Controller.

Figure 51. REFVCC5 Supply Circuit Schematic



8.2.2 Intel® 440BX AGPset Power Management

The Intel® 440BX AGPset supports a variety of system-wide low-power modes using the following functions:

- Hardware interface with the PIIX4E that is used to indicate:
  - — Suspend mode entry
  - — Resume from suspend
  - — Whether to automatically switch from suspend to normal refresh
- Automatic transition from normal to suspend refresh
- Optional automatic transition from suspend to normal refresh
- Optional CPU reset during resume from Power On Suspend (POS)
- Variety of Suspend refresh types:
  - — Self Refresh for SDRAMs
  - — Optional Self Refresh for EDO
  - — Optional CAS Before RAS (CBR) refresh for EDO. An Integrated Ring oscillator is used to provide the time base for the associated logic.

— Programmable slow refresh (relevant for CBR refresh only)

- Isolated I/O pins to significantly reduce power consumption while in POS and STR modes

Based on the above functions, the Intel® 440BX AGPset recognizes the following system-wide low power modes:

- STR and POS suspend entry and exit are generally handled in the same manner. The following exceptions are related to POS mode:
  — The POS resume sequence may or may not include a processor reset. STR, with PCIRST# active always includes a processor reset.
  — The POS resume sequence requires a hardware transition from suspend to a normal refresh. STR with PCIRST# active requires a software initiated transition.
- STD resume is handled in the same way as the power on sequence, including a complete reset of the Intel 440BX AGPset state.

8.2.2.1 System Power Modes

Table 72 provides an overview of how the above features map into system-wide low power modes.

Table 72. System-wide Low-power Modes (Sheet 1 of 2)

System Suspend State	82443BX State	Description	POS Exit PCIRST	External Clk HCLK	External Clk PCLK
Power On	ON	82443BX AGPset is fully on and operating normally. Internal clock gating as well as PCI CLKRUN# may be enabled.	N/A	Active	Active
CPU STOP_GRANT or QUICK_START (C2)	ON	This is transparent to the Intel 82443BX AGPset since the external HCLK and PCLK are unaffected. The Host Bus is Idle. Internal clock gating and PCI CLKRUN# may be enabled.	N/A	Active	Active
CPU STOP CLOCK (C3) (DEEP SLEEP)	POS	System PLLs remain powered, but are disabled. HCLK clock is kept low. The only guaranteed running clock is SUSCLK. The 82443BX maintains DRAM refresh using suspend refresh. The Intel 82443BX's internal PLLs are disabled. The 82443BX PCI and AGP arbiters are disabled.	N	Low	Low or Active

NOTE: The processor will generally be powered off during STR (the processor voltage regulator will be controlled by the PIIX4E's SUSB# signal). In this case, the 82443BX Low Power GTL+ supply (VTT and GTL_REF) should also be controlled by SUSB#, and hence be powered off during STR.

Table 72. System-wide Low-power Modes (Sheet 2 of 2)

Power On Suspend (POS)	POS	System PLLs are powered down. The only running clock is the RTC clock and SUSCLK. The 82443BX maintains DRAM refresh using suspend refresh. The 82443BX's PLLs are disabled. The 82443BX PCI and AGP arbiters are disabled. When resumed, the 82443BX may or may not generate a processor reset. All 82443BX logic, with the exception of resume and refresh, are inactive.	Y	Low	Low
Suspend to RAM (STR)	POS	The processor and other components (with the exception of the DRAM and PIIX4E resume logic) are assumed to be powered OFF. The 82443BX V_{CC} supply is on and all I/O buffers are isolated (with the exception of suspend and DRAM signals). The 82443BX Low Power GTL+ supplies should be powered down with the processor. The 82443BX maintains DRAM refresh using a suspend refresh. All 82443BX logic, with the exception of resume and refresh, are inactive.	Y	Low	Low
Suspend -to-Disk (STD) or Powered-Off	OFF	The entire system is powered OFF except for the PIIX4E resume and RTC wells. Upon resume, the 82443BX resets its entire state.	N/A	X	X

NOTE: The processor will generally be powered off during STR (the processor voltage regulator will be controlled by the PIIX4E's SUSB# signal). In this case, the 82443BX Low Power GTL+ supply (VTT and GTL_REF) should also be controlled by SUSB#, and hence be powered off during STR.

8.2.2.2 System Power-up Sequencing

The waveforms in Figure 52 show the powerup sequence and timing information for the Intel® 440BX AGPset. Table 73 indicates the system power-up sequencing tolerances.

Figure 52. System Power-up Sequencing

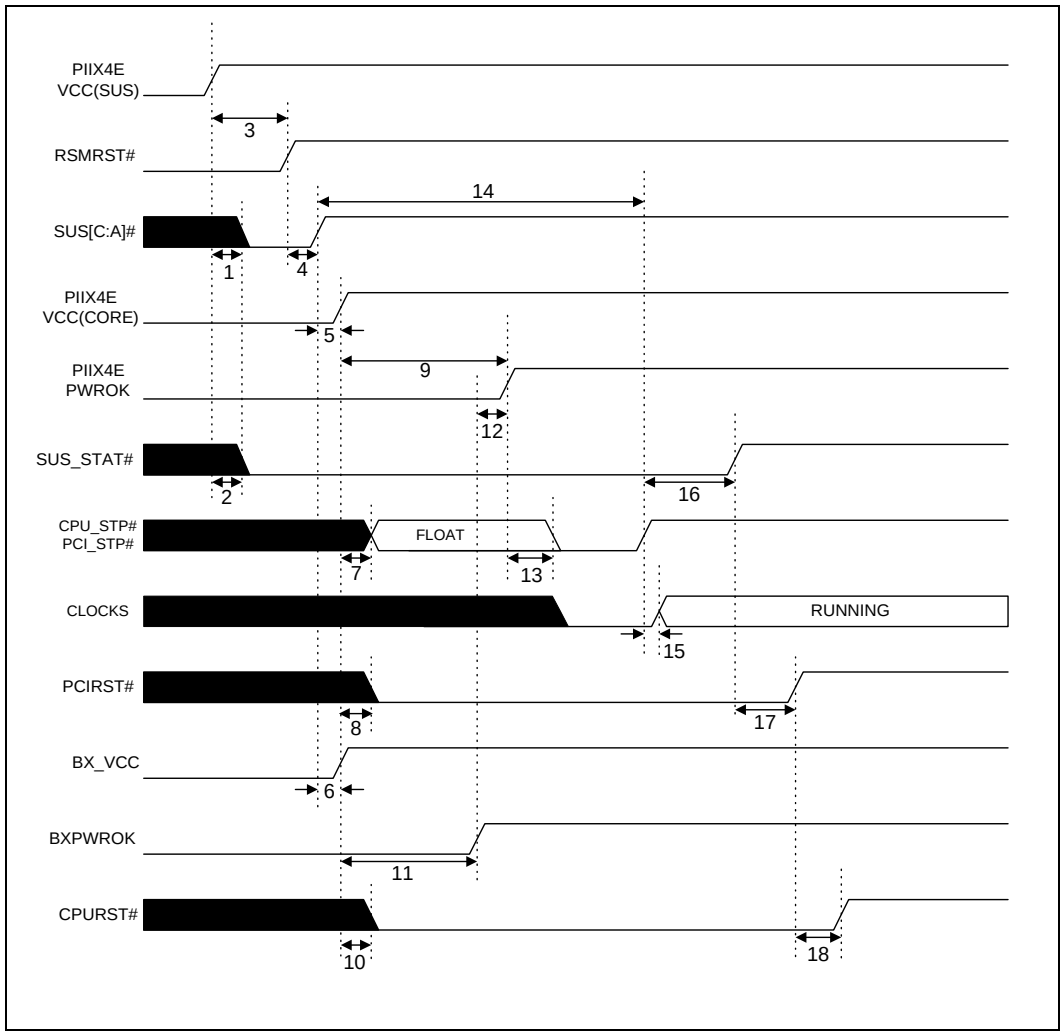


Table 73. System Power-up Sequencing Tolerances

Sym	Parameter	Min	Max	Units	Notes
t_1	PIIX4E VCC(SUS) nominal to SUS[C:A]# active		1	RTC	1
t_2	PIIX4E VCC(SUS) nominal to SUS_STAT[2:1]# active		1	RTC	1
t_3	PIIX4E VCC(SUS) nominal to RSMRST# active	1		ms	
t_4	RSMRST# inactive to SUS[C:A]# inactive	1	2	RTC	1
t_5	SUS[B]# inactive to PIIX4E VCC(CORE) nominal	0		ms	
t_6	SUS[C]# inactive to BX_VCC nominal	0		ms	
t_7	PIIX4E VCC(CORE) nominal to CPU_STP#, PCI_STP# float		1	RTC	1
t_8	PIIX4E VCC(CORE) nominal to PCIRST# active		1	RTC	1
t_9	PIIX4E VCC(CORE) nominal to PIIX4E PWROK active	1		ms	
t_{10}	BX_VCC nominal to CPURST# active		10	ns	
t_{11}	BX_VCC nominal to BXPWROK active	1		ms	
t_{12}	BXPWROK active to PIIX4E PWROK active	0		ns	2
t_{13}	PIIX4E PWROK active to CPU_STP#, PCI_STP# active		1	RTC	1
t_{14}	SUS[C:A]# inactive to CPU_STP#, PCI_STP# inactive	16		ms	3
t_{15}	CPU_STP#, PCI_STP# inactive to clocks running		2	PCICLK	
t_{16}	CPU_STP#, PCI_STP# inactive to SUS_STAT[2:1]# inactive	1		ms	
t_{17}	SUS_STAT[2:1]# inactive to PCIRST# inactive		1	RTC	1
t_{18}	PCIRST# inactive to CPURST# inactive	1		ms	

NOTES:
1. One RTC unit is approximately 32 µs
2. This parameter only applies if BXPWROK will not transition to an active state within 15 ms of SUS[C:A]# de-assertion
3. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL lock and PIIX4 PWROK to be active. When PWROK goes active after 16 ms from SUS[C:A]# inactive, the transition will occur a minimum of one RTC period from PWROK active.

8.2.2.3 Suspend Resume Protocols

The suspend resume sequences are indicated to the 82443BX by the PIIX4E, using SUS_STAT# and PCIRST#. In addition, the 82443BX contains NREF_EN and CRst_En configuration bits that participate in the suspend resume sequences.

As a result of suspend resume, the 82443BX performs the following activities:

- Changing its refresh mode
- Performing internal and processor reset
- Isolate or re-enable normal IO buffers

Table 74 indicates the suspend resume events and activities.

Table 74. Suspend Resume Events And Activities

SUSSTAT#	PCIRST#	CrstEn	Reset	Refresh	I/O Buffers
Assert	Inactive	-	-	Switch to suspend refresh	Isolate
Deassert	Active	-	Reset exclude resume/ref logic	Suspend refresh NREF_EN remains inactive	Enable
Deassert	Inactive	0	No resets	Auto switch to normal ref NREF_EN is set	Enable
Deassert	Inactive	1	Reset processor only	Auto switch to normal ref NREF_EN is set	Enable

The requirements for suspending the 82443BX are:

- The system must be idle when SUS_STAT# is asserted. There must be no active processor or bus masters' cycles and there must be no meaningful pending cycle's information in a chipset or peripheral device's buffers.
- After the assertion of SUS_STAT#, the PIIX4E provides the 82443BX 32 µs with stable power and clocks to perform the necessary suspend sequence.
- The PCICLK must not be stopped with CLKRUN# during the suspend sequence.
- The 82443BX isolates its IO buffers within less than 32 µs time allocated from SUS_STAT# assertion.
  - The 82443BX does not isolate PCIRST# (being pulled up) or clock inputs. The clock inputs are driven low by the clock synthesizer, and 32 µs later the clock synthesizer device may be powered down.

The requirements for resuming the 82443BX are:

- Power and clocks must be stable for at least 1 ms before SUS_STAT# is deasserted.
- When resuming from POS, STPCLK# remains active for about 100 µs after SUS_STAT# deassertion, to allow an automatic switch to normal DRAM operation before processor pending cycles take place.

The 82443BX provides isolation of its I/O buffers during POS and STR. During the events that were specified in Table 74, the isolation takes effect. Table 75 provides information about the state of each of the 82443BX signals during POS and STR.

Table 75. Intel® 440BX AGPset Signal States During POS and STR Modes (Sheet 1 of 2)

Signal Name	State During POS/STR
CPURST#	Three-state
A[31:3]#	Three-state
HD[63:0]#	Three-state
ADS#	Three-state
BNR#	Three-state
BPRI#	Three-state
DBSY#	Three-state
DEFER#	Three-state
DRDY#	Three-state
HIT#	Three-state
HITM#	Three-state
HLOCK#	
HREQ[4:0]#	Three-state
HTRDY#	Three-state
RS[2:0]#	Three-state
RASA[5:0]# / CSA[5:0]#	High1
RASB[5:0]# / CSB[5:0]#	High1
CKE[3:2] / CSA[7:6]#	Low/High2
CKE[5:4] / CSB[7:6]#	Low/High2
CASA[7:0]# / DQMA[7:0]#	High1
CASB[5,1]# / DQMB[5,1]#	High1
GCKE / CKE1	Low/High2
SRAS[B:A]#	Low/High2
CKE0 / FENA	Low/High2
SCAS[B:A]#	High/Low2
MAA[13:0]	Driven3
MAB[9:7]# / MAB[13,10]	Driven3
MAB[12:11]#	Driven3
MAB[6:0]#	Driven3
WEA#, WEB#	High
MD [63:0]	Driven3
MECC[7:0]	Driven3
AD[31:0]	Low
DEVSEL#	Three-state
FRAME#	Three-state
IRDY#	Three-state
C/BE[3:0]#	Low
PAR	Low
PLOCK#	Three-state

NOTES:
1. SDRAM Mode: After putting the SDRAMs into self-refresh mode, these signals are driven high. EDO Mode: For self-refresh mode, RAS and CAS are driven low. Otherwise, the 82443BX continues to refresh during the POS/STR state.
2. SDRAM Mode: SRAS#, SCAS#, CKE[5:0] and GCKE are driven to the first value listed. EDO Mode: These signals are driven to the second value listed.
3. MA lines are always driven by the 82443BX, except for MAB[13:11,9:0]# and MAB10, which are three-stated during reset. MD/MECC are always driven by the 82443BX when there is no active cycle. The values driven on MA, MD and MECC are indeterminate during and after reset.

Table 75. Intel® 440BX AGPset Signal States During POS and STR Modes (Sheet 2 of 2)

Signal Name	State During POS/STR
TRDY#	Three-state
SERR#	Three-state
STOP#	Three-state
PHOLD#	Three-state
PHLDA#	Three-state
WSC#	Three-state
PREQ[4:0]#	Three-state
PGNT[4:0]#	Three-state
PIPE#	Three-state
SBA[7:0]	Three-state
RBF#	Three-state
ST[2:0]	Low
AD_STBA	Three-state
AD_STBB	Three-state
SB_STB	Three-state
G_FRAME#	Three-state
G_IRDY#	Three-state
G_TRDY#	Three-state
G_STOP#	Three-state
G_DEVSEL#	Three-state
G_REQ#	Three-state
G_GNT#	Three-state
G_AD[31:0]	Low
G_C/BE[3:0]#	Low
G_PAR	Low
HCLKIN	
PCLKIN	
DCLKO	Low
DCLKRD	
DCLKWR	
CRESET#	Three-state
PCIRST#	
GCLKIN	
GCLKO	Low
TESTIN#	
SMBCLK	Three-state
SMBDATA	Three-state
CLKRUN#	Three-state
SUSTAT#	

NOTES:

1. SDRAM Mode: After putting the SDRAMs into self-refresh mode, these signals are driven high. EDO Mode: For self-refresh mode, RAS and CAS are driven low. Otherwise, the 82443BX continues to refresh during the POS/STR state.
2. SDRAM Mode: SRAS#, SCAS#, CKE[5:0] and GCKE are driven to the first value listed. EDO Mode: These signals are driven to the second value listed.
3. MA lines are always driven by the 82443BX, except for MAB[13:11,9:0]# and MAB10, which are three-stated during reset. MD/MECC are always driven by the 82443BX when there is no active cycle. The values driven on MA, MD and MECC are indeterminate during and after reset.

8.2.2.4 82443BX Suspend/Resume Sequences and Timing

Table 76 indicates the suspend/resume timing tolerances for Figure 53 through Figure 56.

Table 76. Suspend/Resume Timing Tolerances

Sym	Parameter	Min	Max	Unit
t1	BX_VCC stable to BXPWROK asserted. †	1		ms
t2	BXPWROK asserted to SUS_STAT# inactive	1		ms
t3	Clocks running to SUS_STAT# inactive, ensure	1		ms
t4	BX_VCC active and BXPWROK inactive to CPURST# active		10	ns
t5	SUS_STAT# deasserted to PCIRST# de-asserted, ensure		32	µs
t6	PCIRST# deasserted to CPURST# deasserted	1		ms
t7	SUS_STAT# deasserted to buffers valid	2		HCLK
t8	SUS_STAT# asserted to clocks stopped, ensure	32		µs
t9	SUS_STAT# asserted to suspend refresh		32	µs
t10	SUS_STAT# asserted to buffers isolated		32	µs
t11	PCIRST# asserted to CPURST# asserted		10	ns
t12	PCIRST# asserted to SUS_STAT# de-asserted, ensure	1		ms
t13	SUS_STAT# de-asserted to normal refresh		32	µs
t14	SUS_STAT# de-asserted to CPURST# asserted	0	4	HCLK
t15	CPURST# pulse width	1		ms

† “BX_VCC stable” means BX_VCC is within the specified Functional Operating Range.

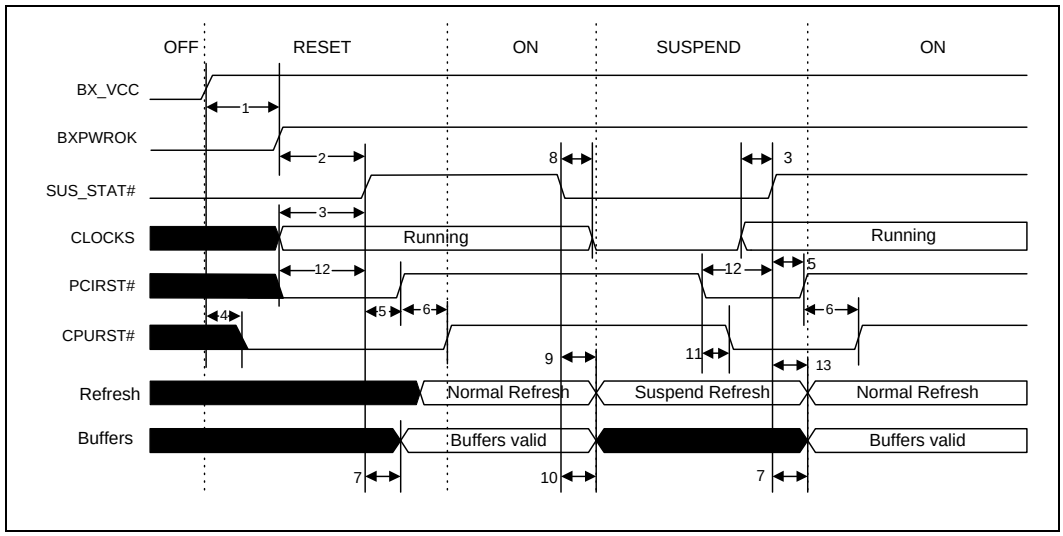
8.2.2.5 Suspend/Resume with PCIRST# Active

The following resume sequence is typically used when resuming from STR. It includes the following components:

- BXPWROK must transition from inactive (low) to active (high) a minimum of 1 ms after BX_VCC is within the specified Functional Operating Range.
- When 15 ms or more may elapse from the time that the PIIX4E deasserts SUS[C:A]# until BXPWROK is asserted, BXPWROK must be asserted before or simultaneous to PWROK being asserted to the PIIX4E.
- Upon resume, the 82443BX detects that the PCIRST# signal is active (low) and drives CPURST# to the processor. Note that CPURST# is driven active based on PCIRST# timing, independent of SUS_STAT# timing.
- Based on the assertion of SUS_STAT#, the 82443BX isolates its I/O buffer within 32 µs.
- Based on the deassertion of SUS_STAT#, the 82443BX enables its I/O buffer to normal operation within 32 µs. Clock inputs and PCIRST# are never gated by the 82443BX and thus affect it before the deassertion of SUS_STAT#.
- Software must release the memory controller from its suspend refresh state to its normal refresh state.
- The 82443BX clears its internal state, with the exception of resume/refresh logic, since it sampled PCIRST# asserted.

Figure 53 shows the suspend resume sequence with PCIRST# active.

Figure 53. Suspend/Resume with PCIRST# Active



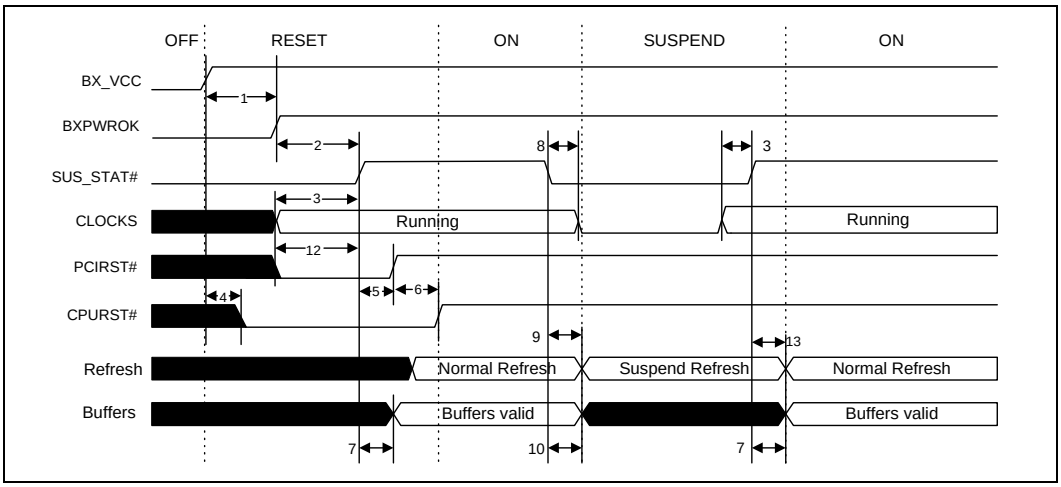
8.2.2.6 Suspend/Resume with CPURST#, PCIRST# Inactive

The following resume sequence is typically used when resuming from POS. It includes the following components:

- Since PCIRST# signal is inactive, per resume the 82443BX does not drive CPURST# to the processor, since CrstEn is '0'.
- Based on the assertion of SUS_STAT#, the 82443BX isolates its I/O buffer within 32 µs.
- Based on the deassertion of SUS_STAT#, the 82443BX enables its I/O buffer to normal operation within 32 µs.
- The 82443BX switches from suspend refresh to normal DRAM operation mode.
- The processor starts execution from the instruction just prior to the stop grant request being recognized. The 82443BX switches to normal DRAM operation before the deassertion of STPCLK#.
- The 82443BX state is not reset.

Figure 54 shows the suspend/resume sequence with CPURST#, PCIRST# inactive.

Figure 54. Suspend/Resume with CPURST#, PCIRST# Inactive



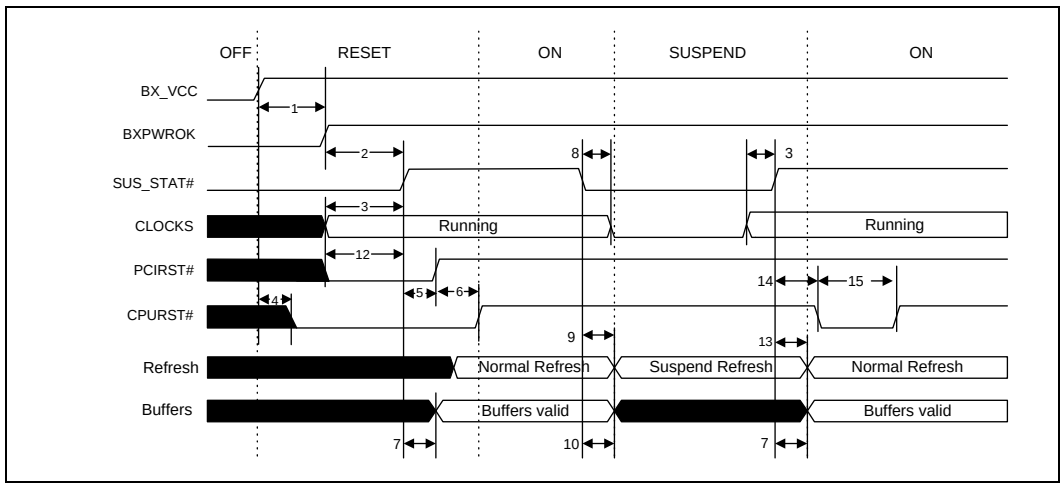
8.2.2.7 Suspend/Resume with CPURST Active, PCIRST# Inactive

The following resume sequence is typically used when resuming from POS. It includes the following components:

- The PCIRST# signal is inactive, upon resume the 82443BX drives CPURST# to the processor since CrstEn is ‘1’. CPURST# is active for 1 ms.
- Based on the assertion of SUS_STAT#, the 82443BX isolates its I/O buffer within 32 µs.
- Based on the deassertion of SUS_STAT#, the 82443BX enables its I/O buffer to normal operation within 32 µs.
- The 82443BX automatically switches from suspend refresh to normal DRAM operation mode when SUS_STAT# deassertion is detected.
- The 82443BX state is not reset.

Figure 55 shows the suspend/resume sequence with CPURST# active, PCIRST# inactive.

Figure 55. Suspend/Resume with CPURST# Active, PCIRST# Inactive



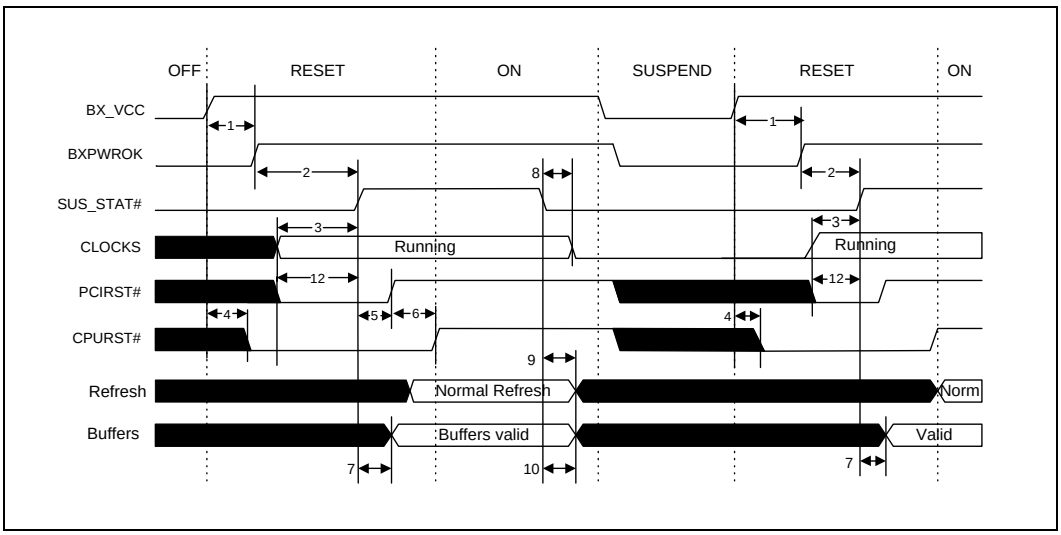
8.2.2.8 Suspend/Resume from STD

The following resume sequence is typically used when resuming from STD. It includes the following components:

- When BXPWROK is sampled low ‘0’, the 82443BX undergoes a complete reset and asserts CPURST#.
- Based on the deassertion of SUS_STAT#, the 82443BX enables its buffer to normal operation within less than 32 µs. Clock inputs and PCIRST# are never gated by the 82443BX and thus affect it before the deassertion of SUS_STAT#.
- Software must release the memory controller from its suspend refresh state to its normal refresh state, and enable refresh with the appropriate refresh rate.

Figure 56 shows the suspend/resume sequence from STD.

Figure 56. Suspend/Resume from STD



Appendix A Bill of Materials

Table 77 is the bill of materials for the Intel® Pentium® III processor — Low Power/440BX AGPset Reference Design.

Table 77. Bill of Materials (Sheet 1 of 8)

Rev. A0

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments	Alternate Manufacturing Info
J14, J15	Conn, Jumper2,1X2 25-mil sq/ 100-mil space, HDR2	3M	929647-09-02		
J20-24	Conn, Jumper3,1X3 25-mil sq/ 100-mil space, HDR3	3M	929647-09-03		
J12	Conn, Fan	AMP	173981-3		
XU9	PLCC, Socket 28	AMP	822271-1		
U6	IC, Clock Generator, CK100, SSOP300-48(PIN)	Cypress	CY2280PVC-11S		
U16	IC, Clock Buffer, 18 Output low skew, SSOP300-48(PIN)	Cypress	CY2318ANZPVC-1		
Y2	Crystal, 32.768KHz, XTAL/MC-405	Epson	MC-405		
J4	Conn, Serial Stack, DB9MX2	FOXCONN	DM10156-73		
J3	Conn, DB25, DB25FM1	FOXCONN	DT11323-R5T		
J7, J8, J9	Conn, PCI Edge Recept., 145154-120	FOXCONN	EH06001-PC-W		
J5, J6	Conn, ISA Edge Recept., isa-98	FOXCONN	EQ04901-S6		
JP1	Conn, Floppy, 17X2 Header	FOXCONN	HL07173-P4		
JP3, JP4	Conn, IDE, 20X2 Header	FOXCONN	HL07206-D2		
J11	Conn, Power, 5566DP-20/ATX	FOXCONN	HM20100-P2		
J1	Conn, PS2 Keyboard / Mouse Connector	FOXCONN	MH11067-D2		
J13	Conn, AGP Edge Recept., 120 pins, AGP-124	FOXCONN	PC1243K-10		
J2	2 USB Stack Connectors	FOXCONN	UB1112C-D3		
U11	BIOS FLASH Memory, TSOP12X20/40S	INTEL	E28F004B5T60		
U8	VLSI, PIIX4, PCI to IDE and ISA Bridge, 324 mBGA, BGA20x20-324	Intel	FW82371EB		
C99, C100, C132, C133,	Chip Capacitor, 10pF, 50 V, CC0603	Kemet	C0603C100J5GAC		

Table 77. Bill of Materials (Sheet 2 of 8)

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Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments	Alternate Manufacturing Info
C22, C42-43, C48-49, C54, C59-65, C70-71, C73, C75-76, C85-87, C90-92, C96-97, C102, C106-108, C111-112, C114, C116-118, C126-127, C129-131, C142, C147, C157, C159-162, C174-176, C181-183, C187-200, C205-206, C208, C226-228	Chip Capacitor, 0.1 uF, 16 V, CC0603	Kemet	C0603C104K4RAC	DO NOT POPULATE C143, C146, C203, C210, C215	
C27-C41, C44-C47, C50-C53	Chip Capacitor, 470 pF, 50 V, CC0603	Kemet	C0603C471K5RAC		
C3-5, C8, C55-57, C94, C119-121, C134, C138, C145, C153	Cap, Tant, 10 uF, 15 V, C Case, 6032	Kemet	T491C106K016AS		
C93, C103-105, C128, C152, C154-156	Cap, Tant, 47 uF, 20 V, D Case, 7343	Kemet	T491D476M020AS		
C2, C6, C58, C72, C84, C88, C89, C95, C109	Cap, Tant, 100 uF, 10 V, D Case, 7343	Kemet	T495D107M010AS		
C1, C7, C23, C66-C68, C74, C77-C82, C101, C113, C115, C141, C158, C163-173, C177-180, C184-186, C201-202, C204,C207, C211-213, C216-217, C220-C225	Chip Capacitor, 0.01 uF 50 V, CC0603	Kemet	C0603C103J5RAC		
U9	IC, PLD, PLCC28, Socket28	LATTICE	GAL22V10B-7LJ		
U23	IC, Linear Voltage Regulator, SOT-223	Linear Tech.	LT1117-3.3cst		

Table 77. Bill of Materials (Sheet 3 of 8)

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Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments	Alternate Manufacturing Info
U5	IC, Linear Voltage Regulator, SOT-223	Linear Tech.	LT1117CST		
XU11	40TSOP BIOS Socket, TSOP12X20/40S	Meritec	980020-40-01		
XU12, XU13	TIL311 SOCKET, DIP14	MILLMAX	110-99-314-41-001		
U25	IC, Logic, 74ACT05, SO14	Motorola	MC74ACT05DR		
FB1-FB-4, FB9	Ferrite Bead, SM1806, Z-Bead	Murata	BLM41P750S		
FB5, FB6, FB7, FB8	Ferrite Bead, SM1806, Z-Bead	Murata	BLM41A800S		
U22	IC, Logic, 74ALS00, SOIC14	National	DM74ALS00M		
U7	IC, Transceiver, 8-Bit Bidirectional Buffer, SOIC20, SO20W	National	DM74ALS245AWM		
C69, C83, C98, C110	Cap, Electrolytic, 220 uF, 25 V, 6.3 mm x 11.2 mm, PCAPR200-300	Panasonic	ECE-A1EU221		
R48, R52, R98-R100, R106, R108-R116, R118-R122	Chip Resistor, 0 Ohm Shunt, 5%, CR0805	Panasonic	ERJ6GEY0R00V		
R25, R42, R45, R49, R63, R101, R102	Chip Resistor, 1 K, 5%, CR0805	Panasonic	ERJ6GEYJ102V		
R2, R4, R5, R11, R40, R41, R43, R53-R56, R105, R117, R123-124, R127	Chip Resistor, 10 K, 5%, CR0805	Panasonic	ERJ6GEYJ103V		
R1, R3, R88, R89, R90, R91	Chip Resistor, 15 K, 5%, CR0805	Panasonic	ERJ6GEYJ153V		
R9, R24	Chip Resistor, 22, 5%, CR0805	Panasonic	ERJ6GEYJ220V		
R10, R12, R13, R14, R39, R58, R70	Chip Resistor, 220, 5%, CR0805	Panasonic	ERJ6GEYJ221V		
R92-R95	Chip Resistor, 27, 5%, CR0805	Panasonic	ERJ6GEYJ270V		
R20, R44, R57, R71	Chip Resistor, 2.7 K, 5%, CR0805	Panasonic	ERJ6GEYJ272V		
R17-R19, R21, R23, R26, R28, R30, R32, R34, R36, R38	Chip Resistor, 33, 5%, CR0805	Panasonic	ERJ6GEYJ330V		
R103,R104	Chip Resistor, 470, 5%, CR0805	Panasonic	ERJ6GEYJ471V		
R7, R64-R69, R125, R126, R128	Chip Resistor, 4.7 K, 5%, CR0805	Panasonic	ERJ6GEYJ472V		
R72-R87, R96, R107	Chip Resistor, 8.2 K, 5%, CR0805	Panasonic	ERJ6GEYJ822V		

Table 77. Bill of Materials (Sheet 4 of 8)

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Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments	Alternate Manufacturing Info
S1, S2	Switch-Push Button, PBSW / PNASNC2	Panasonic	EVQ-PHP03T		
RP2, RP3, RP41-RP47, RP54-RP56, RP58, RP60, RP61	Res, Array, SMT, 33, 5%, EXB-V	Panasonic	EXB33V330JV		
RP10, RP18, RP23	Res, Array, SMT, 1 K, 5%, EXB-V	Panasonic	EXB38V102JV		
RP8-9, RP11, RP13-17, RP19-RP22, RP24, RP26-33, RP35-36, RP39, RP51-52, RP59	Res, Array, SMT, 10 K, 5%, EXB-V	Panasonic	EXB38V103JV		
RP1, RP4	Res, Array, SMT, 22, 5%, EXB-V	Panasonic	EXB38V220JV		
RP25, RP37, RP49, RP50, RP53	Res, Array, SMT, 2.7 K, 5%, EXB-V	Panasonic	EXB38V272JV		
RP57	Res, Array, SMT, 47, 5%, EXB-V	Panasonic	EXB38V470JV		
RP5, RP6, RP7, RP48	Res, Array, SMT, 4.7 K, 5%, EXB-V	Panasonic	EXB38V472JV		
RP12, RP34	Res, Array, SMT, 5.6 K, 5%, EXB-V	Panasonic			
U24	IC, Logic, Inverter, Schmitt Trigger, SOIC14	Philips	74LVC14AD		
U10	IC, Logic, 10 Bit Bus Switch, QSOP, SO24W	Quality Semi	QS3384SO		
Y1	Crystal,14.318 MHz, XTAL, FOX-HC495D	Raltron	AS-14.31818-20		
F1-F3	Fuse, Drawing, SM250	RayChem	SMD250-2		
XBT1	Battery Holder Socket	Renata	HU-2032-1		
BT1	Battery	Reneta	CR2032		
D1, D2, D5	Diode, LED, SOT23-A	Siemens	LGS260-DO		
U1	VLSI, Super I/O, QFP128	SMSC	FDC37B787		
C122-C125	Chip Capacitor, 47 pF, CC0603	TDK	C1608C0G1H470JT $		
C9-C21, C24-C26	Chip Capacitor, 220 pF, CC0603	TDK	C1608X7R1H221KT 009A		
U15	IC, Logic, 3-state buffer, SOP-14	TI	74LVC125A		
U21	IC, Logic, SOP-14	TI	74LVC14A		
U3, U4	IC, RS232 Transceiver, SOIC20, SO20W	TI	GD75232DW		
U2	IC, Logic, Open Drain Buffer, SOP-14	TI	SN7407D		
U12, U13	7 Segment LED display, DIP14	TI	TIL311		
D3-D4, D6-D7	Schottky Diode, SOT23-E	ZETEX	BAT54		

Table 77. Bill of Materials (Sheet 5 of 8)

Rev. A0

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments	Alternate Manufacturing Info
R8, R15, R16, R46, R47	Chip Resistor, 124, 1%, CR0805	Panasonic	ERJ-6ENF1240V		
RP38, RP40	Res, Array, SMT, 270, 5%, EXB-V	Panasonic	EXB38V271JV		
R300-R307	Chip Resistor, 0, 5%, CR0805	Panasonic	ERJ6GEY0R00V		
R50	Chip Resistor, 680, 5%, CR0805	Panasonic	ERJ6GEYJ681V		
R308	Chip Resistor, 33, 5%, CR0805	Panasonic	ERJ6GEYJ330V		
R309	Chip Resistor, 0 Ohm Shunt, 5%, CR0805	Panasonic	ERJ6GEY0R00V		
J25	Conn, ITP, Vertical Recept., 30 pins	AMP	104078-4		
XU28	SPDIP, Socket 28	AMP	345724-1		
C331, C332, C333, C334, C335	Chip Capacitor, 10 uF,16 V, Y5V, CC1210	AVX Corp	1210YG106ZAT4A		
D9, D11	Schottky Diode, SOD-323	Central Semiconductor	CMDSH-3TR		
L2	Inductor, 1uH, IRMS = 12.5 A, ISAT = 15.3 A, DCRmax = .0034 ohm, UNI-PAC 3B	Coiltronics	UP3B-1R0		
L3	Inductor, 2.2 uH, IRMS = 3.1 A, ISAT = 3.5 A, DCRmax = .0363 ohm, UNI-PAC 1B	Coiltronics	UP1B-2R2		
R402	Chip Resistor, 15 milliohms, 5%, CR2512	Dale/Vishay	WSL-2512 0.015 5%		
R329, R403	Chip Resistor, 3 milliohms, 5%, CR2512	Dale/Vishay	WSL-2512 0.003 5%		
Q2, Q3, Q4	N-Channel FET, 25 V, SOT-23	Fairchild	FDV301N		
U33	Dual N Channel MOSFET, SO8	Fairchild	FDS6982		
U27	82443BX Host Bridge/ Controller, 492 BGA	Intel	FW82443BX		
U26	Pentium® III Processor – Low Power at 500 MHz with 256 Kbyte L2 cache, 495 BGA2	Intel	KC80526LY500256		
U34, U35	N Channel MOSFET, SO8	International Rectifier	IRF7809A		
U31	N Channel MOSFET, SO8	International Rectifier	IRF7811A		
C230	Cap, Tant., 33 uF, 16 V, 7343	Kemet	T495D336M016AS		
U32	Dual Regulator Controller, SSOP36	Linear Tech	LT1708PG#TRSL25 026		
U30	Remote/Local Temp Sensor, QSOP16	Maxim	MAX1617MEE		
U28	8-bit CMOS FLASH Microcontroller, SPDIP28	Microchip	PIC16LF873-04I/SP		
L1	Chip Inductor, 4.7 uH, 10%, 30 mA, .7ohm, CR0805	Murata	LQG21N4R7K10		

Table 77. Bill of Materials (Sheet 6 of 8)

Rev. A0

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments	Alternate Manufacturing Info
Y3	Crystal, 4 MHz, +/-0.5%	Murata	CSA4.00MG		
D12	Schottky Barrier Rectifier, 1 A, 40V, 457-04	On Semiconductor	MBRM140T3		
D10	Schottky Barrier Rectifier, 3 V, 40 V, 403-03	On Semiconductor	MBRS340T3		
C350	Cap, SP, 180 uF, 4 V, UE	Panasonic	EEFUE0G181R		
C353, C354, C355, C356	Cap, SP, 270 uF, 2 V, UE	Panasonic	EEFUE0D271R		
C343	Cap, Tant., 4.7 uF, 6.3 V, Y	Panasonic	ECST0JY475R		
C232, C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C295, C296, C305, C306, C307, C308, C309, C310, C312, C313, C314, C315, C316, C317, C318, C319, C323, C327, C328, C336, C338, C358, C359	Chip Capacitor, 0.1 uF, 16 V, X7R, CC0603	Panasonic	ECJ1VB1C104K	For 700MHz processor, populate C238-C245, C297-C299 with .22 uF, X7R, CC 0603: Panasonic ECJ1VB1A224K	
C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276	Chip Capacitor, 0.1 uF, 16 V, X7R, CC0805	Panasonic	ECJ2VB1C104K	For 700MHz processor, populate C250-C276 with 2.2 uF, X5R, CC 0805: Panasonic ECJ2YB0J225K	
C329, C330	Chip Capacitor, 0.1 uF, 25 V, X7R, CC0603	Panasonic	ECJ1VB1E104K		

Table 77. Bill of Materials (Sheet 7 of 8)

Rev. A0

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments	Alternate Manufacturing Info
C337	Chip Capacitor, 0.47 uF, 16 V, X7R, CC0805	Panasonic	ECJ2YB1C474K		
C339, C342, C345, C348	Chip Capacitor, 1000 pF, 50 V, X7R,CC0603	Panasonic	ECJ1VB1H102K		
C347	Chip Capacitor, 100 pF, 50 V, NPO, CC0603	Panasonic	ECUV1H101JCV		
C357	Chip Capacitor, 10 uF, 10 V, X5R, CC1210	Panasonic	ECJ4YB1A106K		
C325, C326	Chip Capacitor, 15 pF, 50 V NP0, CC0603	Panasonic	ECUV1C150JCV		
C341	Chip Capacitor, 180 pF, 50 V, NPO, CC0603	Panasonic	ECUV1H181JCV		
C344	Chip Capacitor, 1 uF, 10 V, X7R, CC0805	Panasonic	ECJ2YB1A105K		
C322	Chip Capacitor, 20 pF, 16 V, NP0, CC0603	Panasonic	ECUV1C200JCV		
C346	Chip Capacitor, 330 pF, 50 V, NPO, CC0603	Panasonic	ECUV1H331JCV		
C349	Chip Capacitor, 33 pF, 50 V, NPO, CC0603	Panasonic	ECUV1H330JCV		
R334, R391	Chip Resistor, 0, 5%, CR0805	Panasonic	ERJ6GEY0R00V		
R327, R333, R359, R360, R383	Chip Resistor, 1.5K, 5%, CR0805	Panasonic	ERJ6GEYJ152V		
R393, R396, R399	Chip Resistor, 10, 5%, CR0805	Panasonic	ERJ6GEYJ100V		
R332, R342	Chip Resistor, 100, 1%, CR0805	Panasonic	ERJ6ENF1000V		
R395	Chip Resistor, 100K, 5%, CR0805	Panasonic	ERJ6GEYJ015V		
R400, R407, R411	Chip Resistor, 10K, 1%, CR0805	Panasonic	ERJ6ENF0014V		
R323, R336, R350, R347, R361, R397, R398, R335, R345	Chip Resistor, 10k, 5%, CR0805	Panasonic	ERJ6GEYJ103V		
R315	Chip Resistor, 110, 1%, CR0805	Panasonic	ERJ6ENF1100V		
R325, R339, R338	Chip Resistor, 150, 1%, CR0805	Panasonic	ERJ6ENF1500V		
R381, R382, R388, R389, R390	Chip Resistor, 150, 5%, CR0805	Panasonic	ERJ6GEYJ151V		
R405	Chip Resistor, 15K, 5%, CR0805	Panasonic	ERJ6GEYJ153V		
R401	Chip Resistor, 160K, 5%, CR0805	Panasonic	ERJ6GEYJ164V		
R324, R326, R331	Chip Resistor, 1K, 1%, CR0805	Panasonic	ERJ6ENF1001V		

Table 77. Bill of Materials (Sheet 8 of 8)

Rev. A0

Reference Designator	Description	Manufacturer	Manufacturer P/N	Comments	Alternate Manufacturing Info
R311, R312, R313, R341, R353, R372, R373, R376, R377, R379, R392, R316, R317, R318, R319	Chip Resistor, 1K, 5%, CR0805	Panasonic	ERJ6GEYJ102V		
R394, R409, R410	Chip Resistor, 1M, 5%, CR0805	Panasonic	ERJ6GEYJ016V		
R344, R340, R343	Chip Resistor, 22, 5%, CR0805	Panasonic	ERJ6GEYJ220V		
R380, R387	Chip Resistor, 240, 5%, CR0805	Panasonic	ERJ6GEYJ241V		
R369, R374	Chip Resistor, 270, 5%, CR0805	Panasonic	ERJ6GEYJ271V		
R330	Chip Resistor, 2K, 1%, CR0805	Panasonic	ERJ6ENF2001V		
R375, R378	Chip Resistor, 3.3K, 5%, CR0805	Panasonic	ERJ6GEYJ332V		
R320	Chip Resistor, 330, 5%, CR0805	Panasonic	ERJ6GEYJ331V		
R408	Chip Resistor, 33K, 5%, CR0805	Panasonic	ERJ6GEYJ333V		
R385, R386	Chip Resistor, 47, 5%, CR0805	Panasonic	ERJ6GEYJ470V		
R314, R328, R384	Chip Resistor, 56.2, 1%, CR0805	Panasonic	ERJ6ENF56R2V		
R406	Chip Resistor, 68K, 5%, CR0805	Panasonic	ERJ6GEYJ683V		
R404	Chip Resistor, 7.5K, 1%, CR0805	Panasonic	ERJ6ENF0752V		
R337	Chip Resistor, 75, 1%, CR0805	Panasonic	ERJ6ENF0750V		
D8	Schottky Diode, SOT23-E	Zetex	BAT54		

Appendix B Schematics

Schematics are provided for the following items listed below. Schematics are available from the Intel Developer's web site in OrCAD* (version 9.0 or later) and PDF format.

- Table of Contents
- Block Diagram
- Routing Requirements
- Pentium® III Processor – Low Power Part 1
  - This design will support either the Pentium® III processor – Low Power or the Intel® Celeron™ processor – Low Power in a 495 BGA2 package.
- Pentium® III Processor – Low Power Part 2
  - When using a processor running at 700 MHz or above, larger value capacitors for high and mid frequency decoupling will be required. A table is provided on this page with the proper stuffing.
- 82443BX Part 1 Host, PCI, and AGP
- 82443BX Part 2 Memory, Power, and GND
- ITP, Thermal Sensor, and Clock Throttling
  - The ITP, thermal sensor chip, and microcontroller are optional. More information on using a microcontroller to throttle the processor may be found in the *Pentium® III Processor Active Thermal Management Technology Application Note* (order number 273405). This application note also contains sample microcontroller code.
- Processor Voltage Regulator
- Mini-PCI Connector (Not Populated)
- DIMM0
  - This design uses DIMMs instead of SO-DIMMs. For DIMM design guidelines, please see the *Intel® 440BX AGPset Design Guid*e (order number 290634). Note also that Suspend To RAM is not supported as the DIMMs are powered with 3.3 V and not 3.3 VSB.
- DIMM1
- DIMM2 (Not Populated)
- System Clocks
  - This design uses a CK100 compatible clock synthesizer instead of a CK100-M or CK100-SM. Because this design uses DIMMs, a CKBF SDRAM buffer is used instead of a CKBF-M.
- PCI/ISA Pullups
- PCI Connectors 0 and 1
- PCI Connector 2
- AGP Connector
- PIIX4E Part 1
- PIIX4E Part 2

- IDE Connectors
- Super I/O
- USB Connectors
- ISA Connectors
- Serial / Parallel / Floppy
- Flash BIOS / Port 80
  - The code for the PLD is in Appendix C.
- ATX Power Connector
- Unused Devices

Intel® Pentium® III Processor - Low Power / 440BX AGPset Reference Design

Revision A0

Table of Contents

Revision History

Aug-24-2001

- Moved location of pull-up resistor on STPCLK# closer to the PIIX4E.

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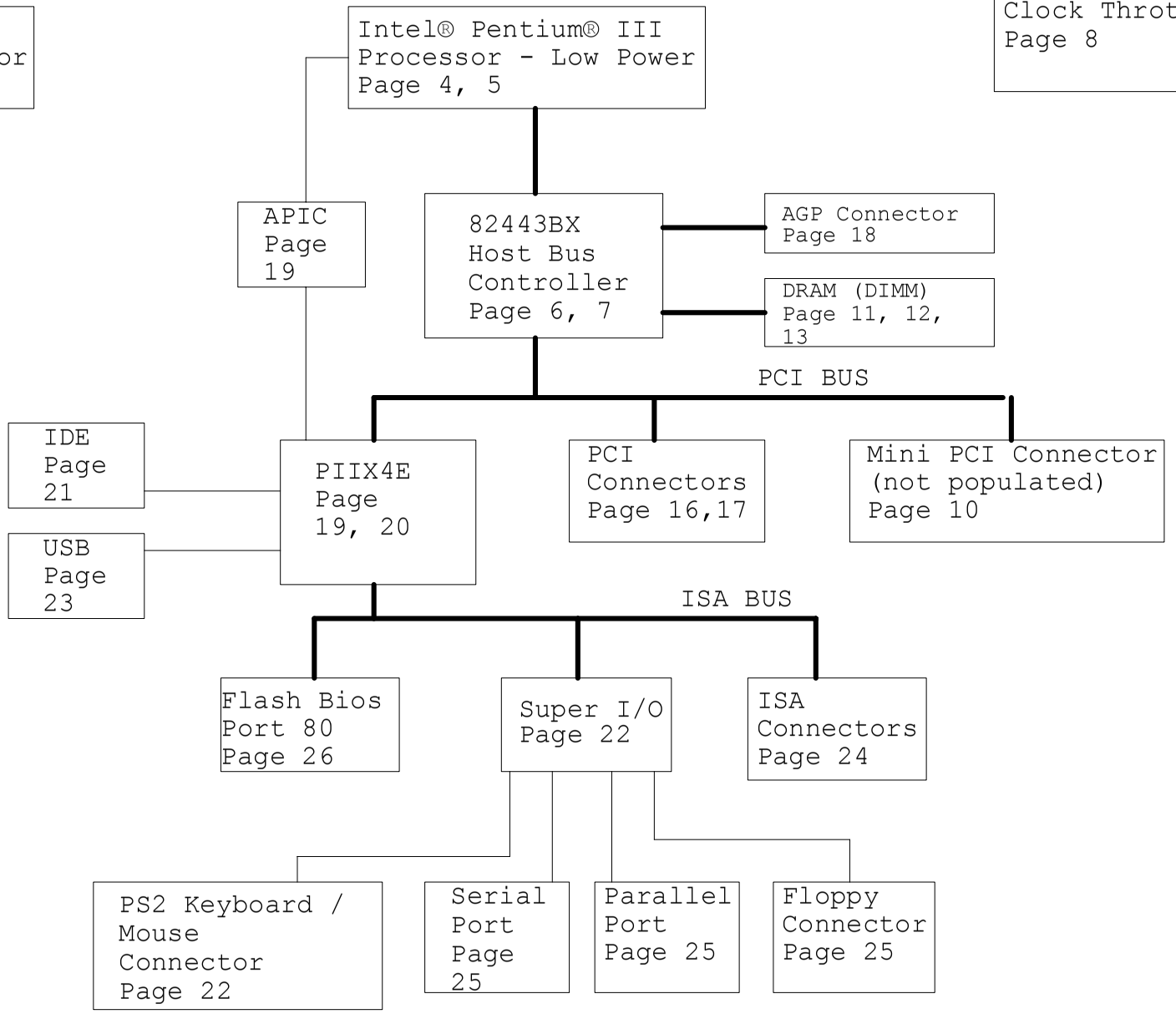
Block Diagram

Optional

ITP Connector
Thermal Sensor
Clock Throttle Controller
Page 8

Processor
Voltage Regulator
Page 9



System Clocks
Page 14

ATX Power
Connector
Page 27

PCI / ISA
Pullups
Page 15

Unused Devices
Page 28

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Routing Requirements

General Board Design Requirements

>> Right angle traces must not be used.
>> Vias for decoupling capacitors must be kept as close as possible to the capacitor pad.
>> Trace impedance must be 65 ohms, +/- 10% unless otherwise noted.
>> GND layers must not be split.
>> Series terminating resistors must be kept as close to the driving pin as possible.
>> Daisy chain signals going to more than one point, do not use stubs.
>> Specific routing requirements are included throughout schematic sheets.

CPU Routing Requirements

>> Consult the Intel® Pentium® III Processor - Low Power/ 440BX AGPset Design Guide for routing requirements for the following GTL+ signals:
BPRI#, DEFER#, HRESET#, RS#[2:0], HTRDY#, H_PRDY#, HA#[31:3], ADS#, BNR#, BREQ0#, HD#[63:0], DBSY#, DRDY#, HIT#, HITM#, HLOCK#, HREQ#[4:0]
>> The capacitor C230 should be close to the PLL1 and PLL2 pins, with less than 0.1ohm per route. The inductor L1 should be close to the capacitor. The PLL2 route should be parallel and next to the PLL1 route (minimize loop area). Any routing resistance should be inserted between VCCT and the inductor. Consult the PLL RLC Filter Specification in the Pentium® III processor - Low Power datasheet to determine if routing resistance is required.
>> Route THERMDP and THERMDN close together as a pair (no more than 250 mil difference in length), on same layer, in parallel, and 25 mils min from any other trace.
>> Route VREF using 24 mil minimum width trace, and separate from all other traces by 25 mils minimum.
>> Place ITP port near the processor. ITP port must be at end of following traces: HRESET#, H_PRDY#, H_TCK, H_TMS. Series termination resistors for HRESET#, H_PRDY#, H_TCK, H_TMS must be placed less than 1" from port.
>> Consult the Decoupling Recommendations in the Intel® Pentium® III Processor - Low Power/ 440BX AGPset Design Guide for processor decoupling capacitor layout recommendations.

Clock Specific Routing Requirements

Note: This design uses a CK100 clock synthesizer.
>> Clocks must be routed on the same layer internally to contain EMI. Space all other signals at least 2W from clock traces.
>> Intel recommends that the clock series resistors not be placed in the R-packs to allow individual tunability if necessary.
>> Minimize via's on all clock traces.
>> Do not allow the clock traces to cross a plane split.
>> CPUCLK0 - Follow host clock layout guidelines in Pentium III processor - Low Power/ 440BX AGPset design guide
>> PCICLK7 should be 0" to 4" greater than the length of CPUCLK0 (from CK100 to 82443BX). PCICLK7 should be the same length as PCICLKF. PCI Clocks PCICLK[4:1] must be matched in length and should equal the length of PCICLK7 - 2.5".
>> GCLKOUT should be less than or equal to 1". GCLK should equal GCLKIN + 3.3"
>> BXDCLKO must be between 1" to 6" in length. All SDRAM clocks SDCLK[11:0] must be matched in length; this length should be between 1" and 3". BxFBCLK must be 2.5" longer that SDCLKx.

IDE Specific Routing Requirements

>> Place IDE series terminating resistors within 1" of PIIX4E.
>> Place IDE connector within 4" of PIIX4E.

Power Supply Specific Routing Requirements

>> All traces associated with the input power/ground connectors, and the capacitors connected to these connectors, must be routed with minimum length and maximum width.
>> All unrelated signals and power planes must be kept away from the switching circuitry.
>> Consult the Voltage Regulator Datasheet for specific routing requirements

Memory Bus Specific Routing Requirements

>> Consult the 440BX Design Guide for DIMM routing guidelines.

PCI Bus Specific Routing Requirements.

>> The PIIX4E must be the last device on the PCI bus.

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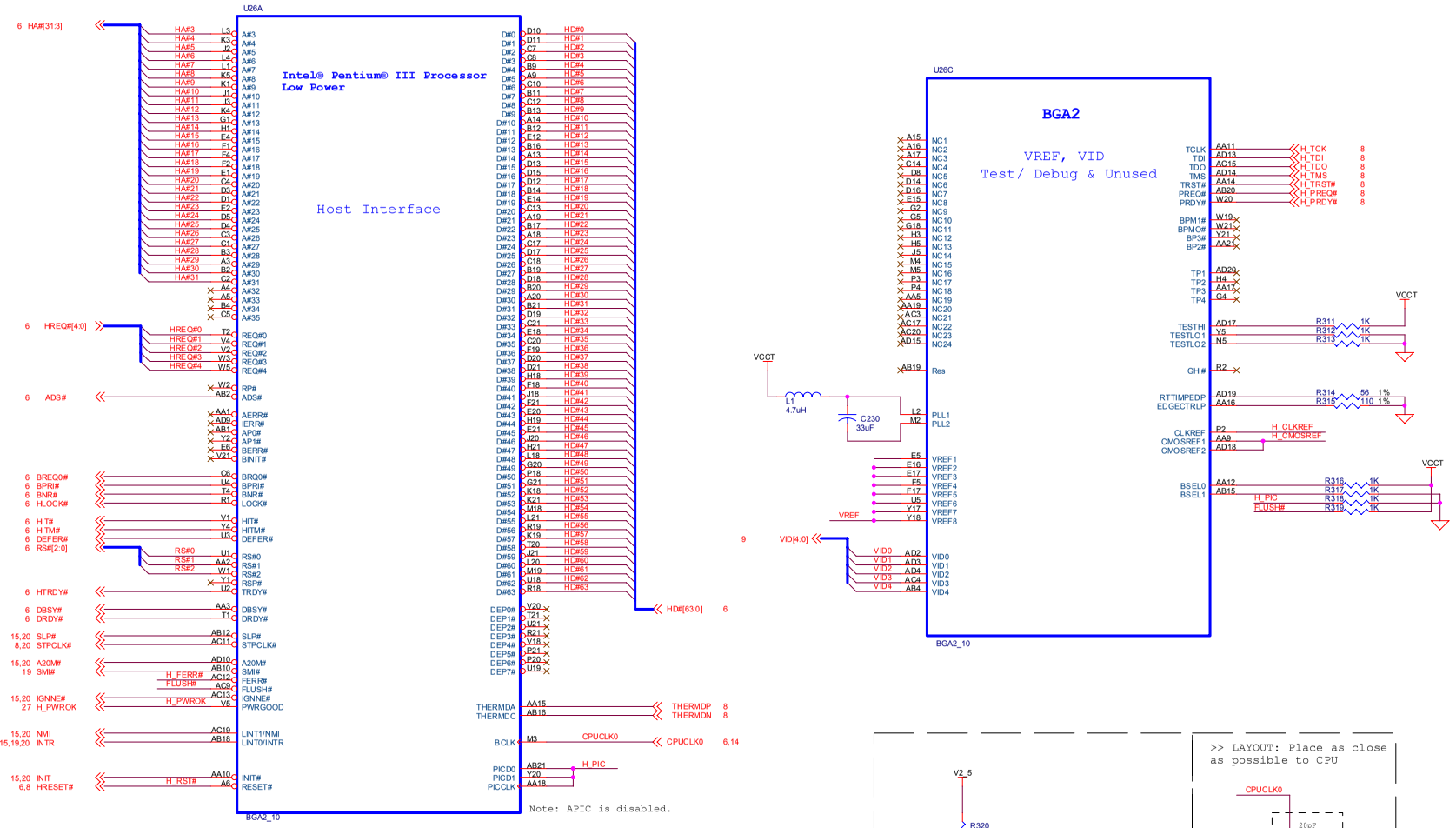
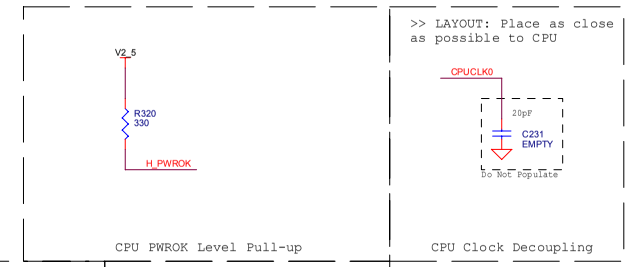
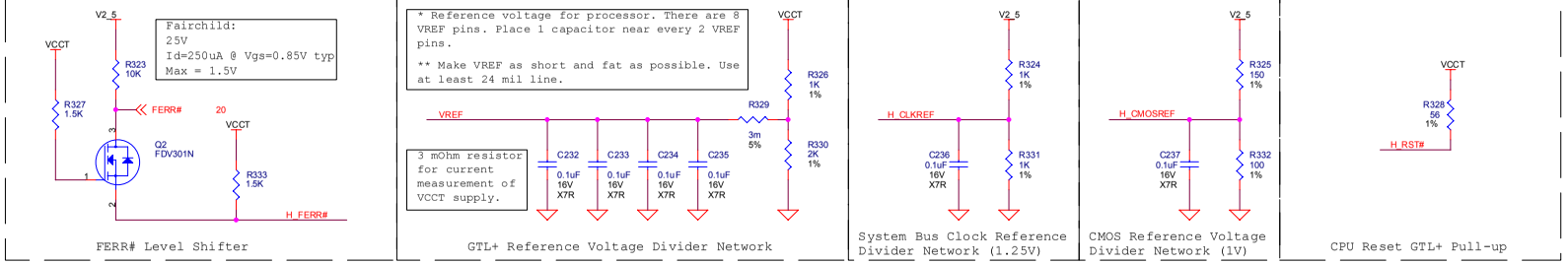
Pentium® III Processor - Low Power Part 1







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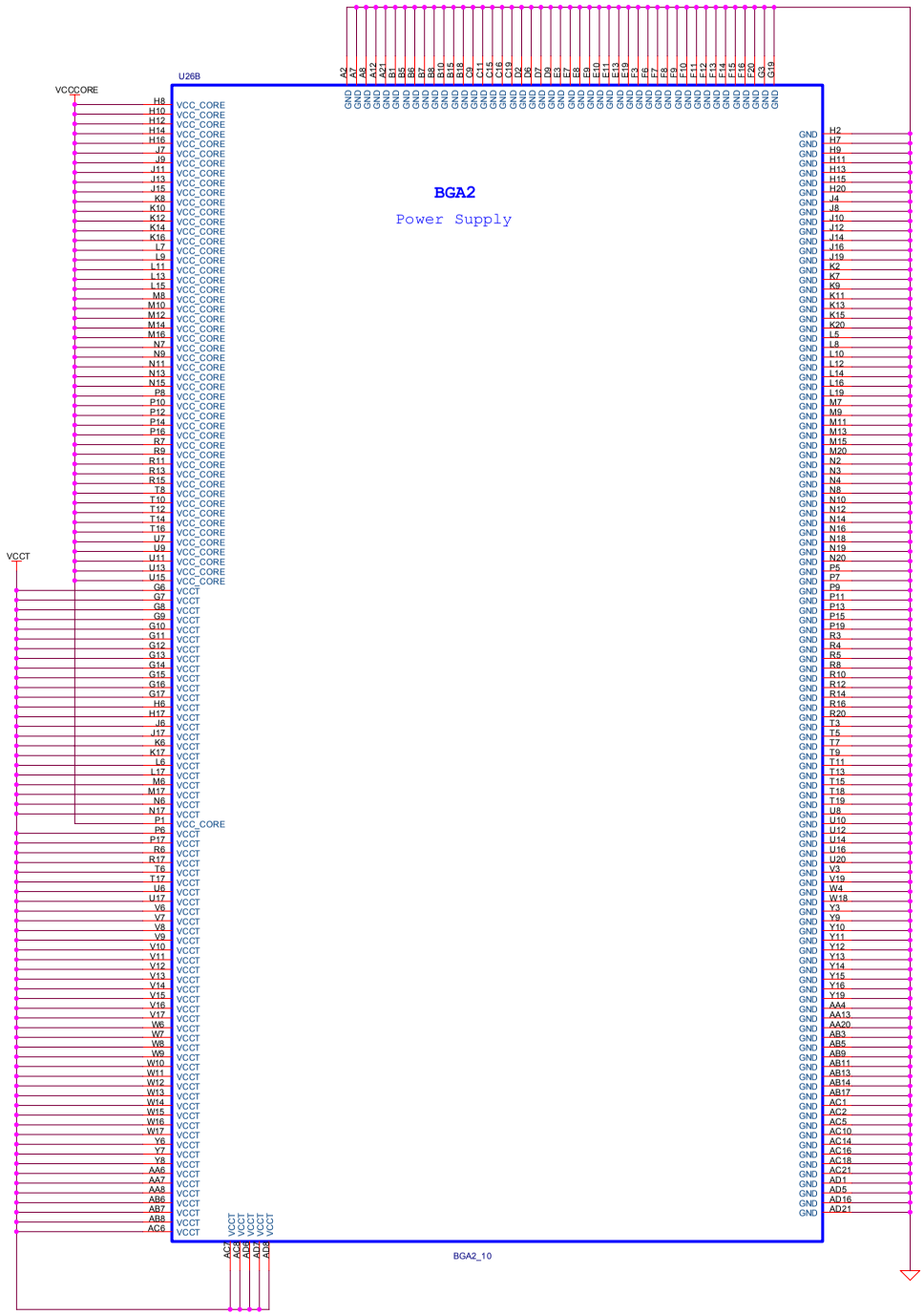
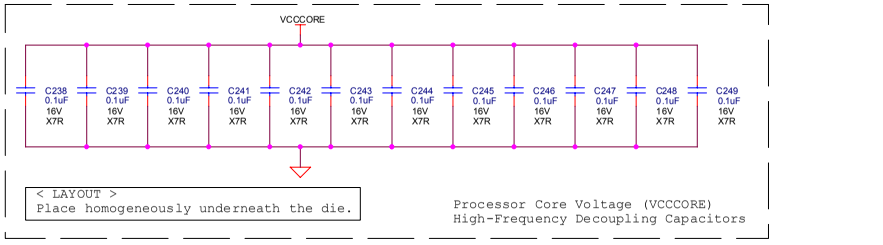
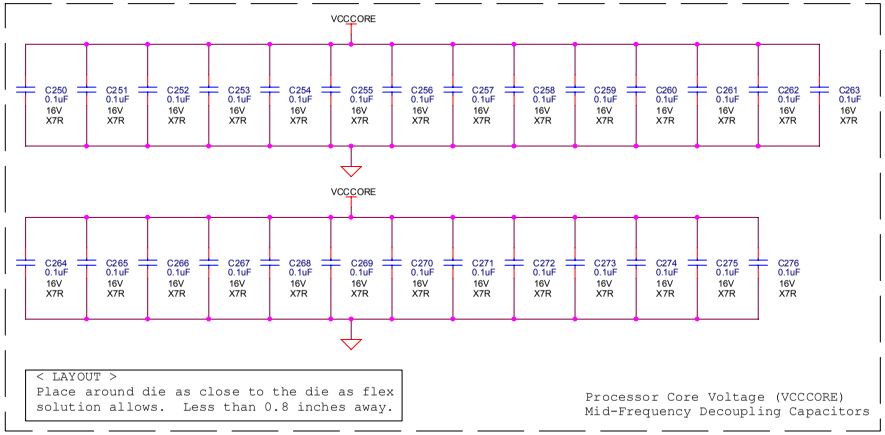
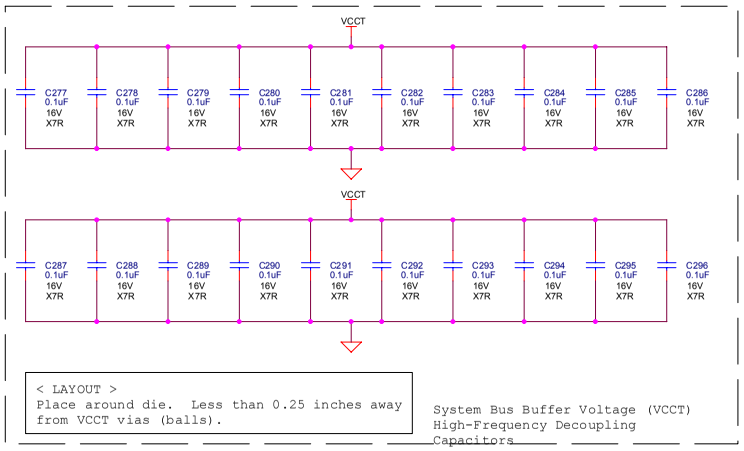
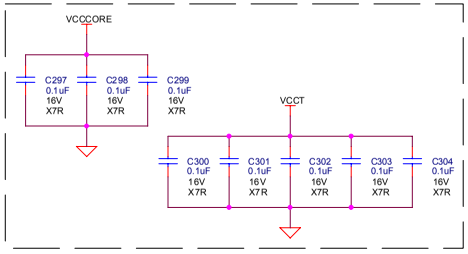
Pentium® III Processor - Low Power Part 2











Decoupling Capacitor	Ref Des	< 700MHz	700MHz
VCCCORE High Freqency	C238-C249	0.1uF	0.22uF
VCCCORE High Freqency	C297-C299	No Pop	0.22uF
VCCCORE Mid Freqency	C250-C276	0.1uF	2.2uF
VCCT High Freqency	C277-C296	0.1uF	0.1uF
VCCT High Freqency	C300-C304	No Pop	No Pop

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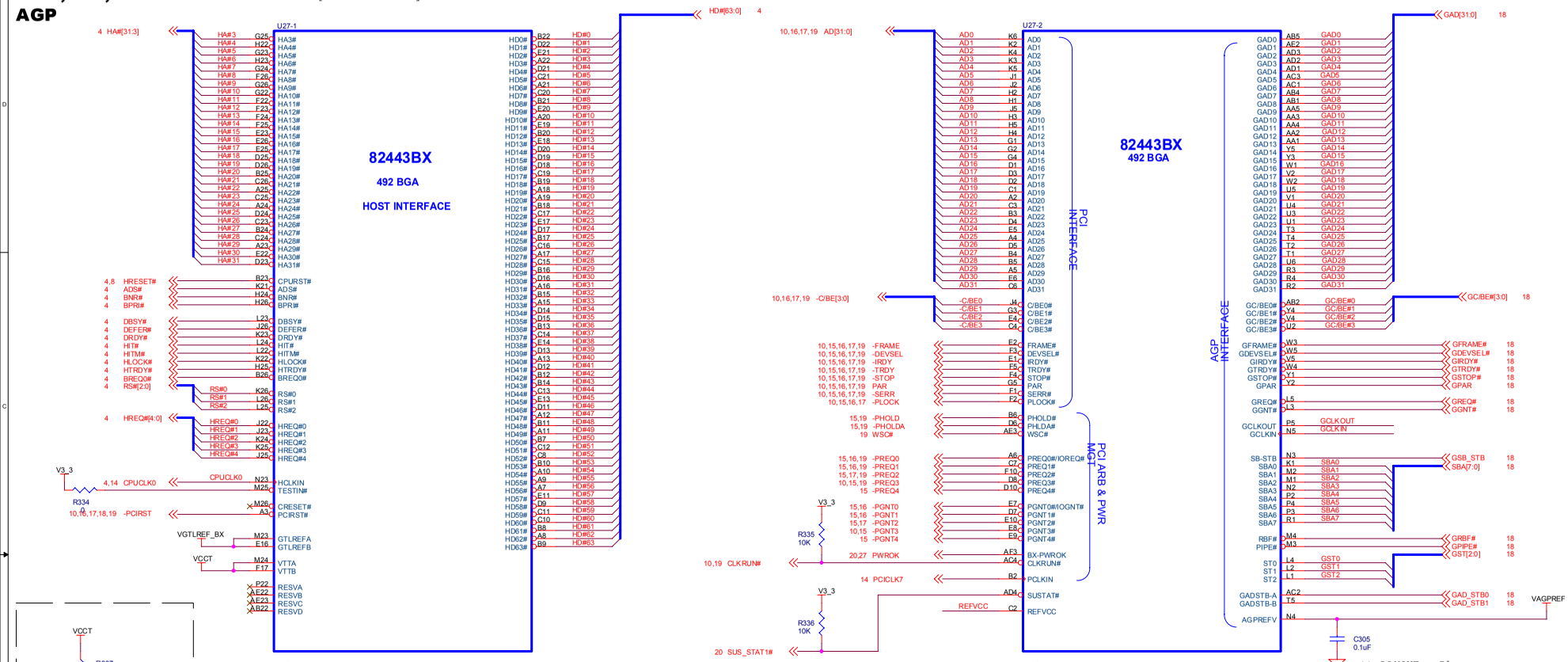
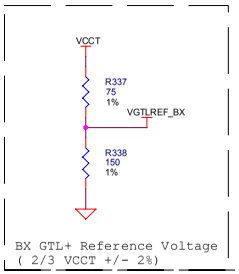
82443BX Part 1 Host, PCI, and AGP

< LAYOUT > Silkscreen
Put 82443BX pin numbers on both
top and bottom layers.





BX GTL+ Reference Voltage
(2/3 VCCT +/- 2%)

>> LAYOUT: Place as close as possible to 82443BX.

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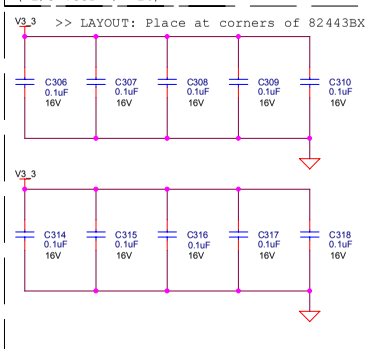
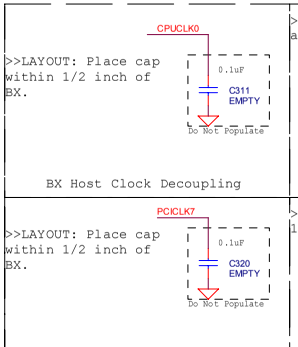
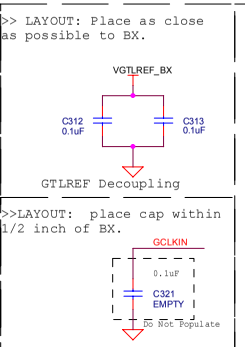


82443BX Power Decoupling Caps



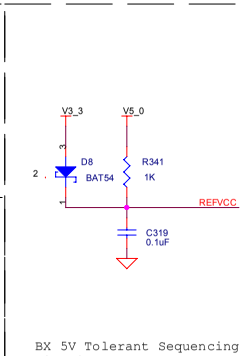
BX Host Clock Decoupling

BX PCI Clock Decoupling

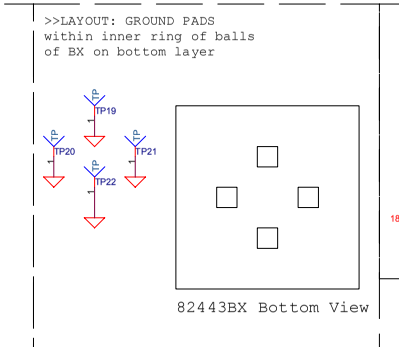


GTLREF Decoupling

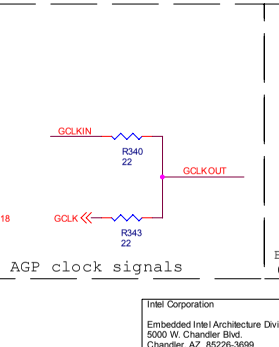
AGP Clock Decoupling



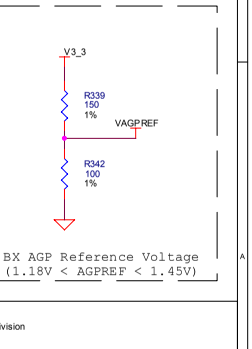
BX 5V Tolerant Sequencing Circuit



82443BX Bottom View



AGP clock signals



BX AGP Reference Voltage
(1.18V < AGPREF < 1.45V)

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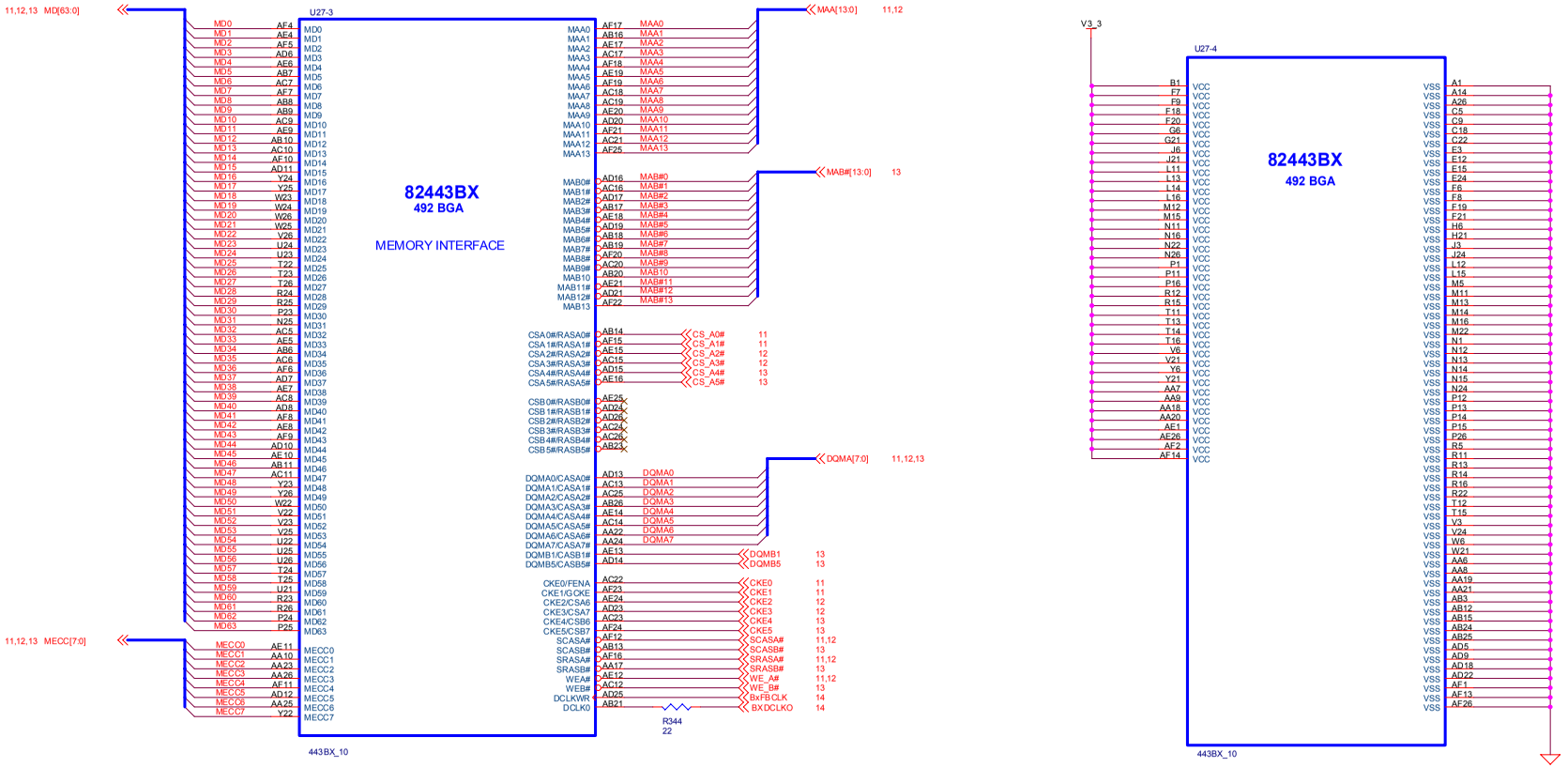
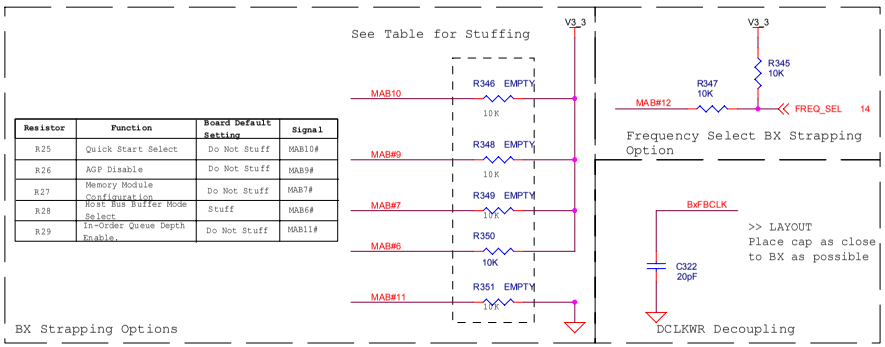
82443BX Part 2
Memory, Power, and GND





Resistor	Function	Board Default Setting	Signal
R25	Quick Start Select	Do Not Stuff	MAB10#
R26	AGP Disable	Do Not Stuff	MAB9#
R27	Memory Module Configuration	Do Not Stuff	MAB7#
R28	Host Bus Buffer Mode Select	Stuff	MAB6#
R29	In-Order Queue Depth Enable.	Do Not Stuff	MAB11#

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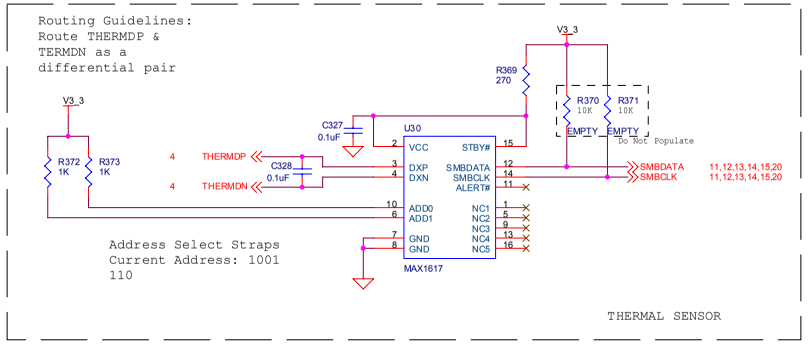
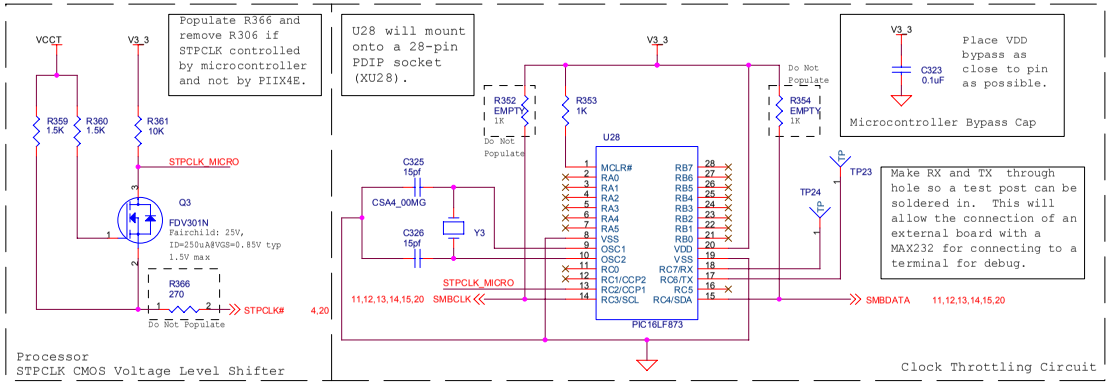
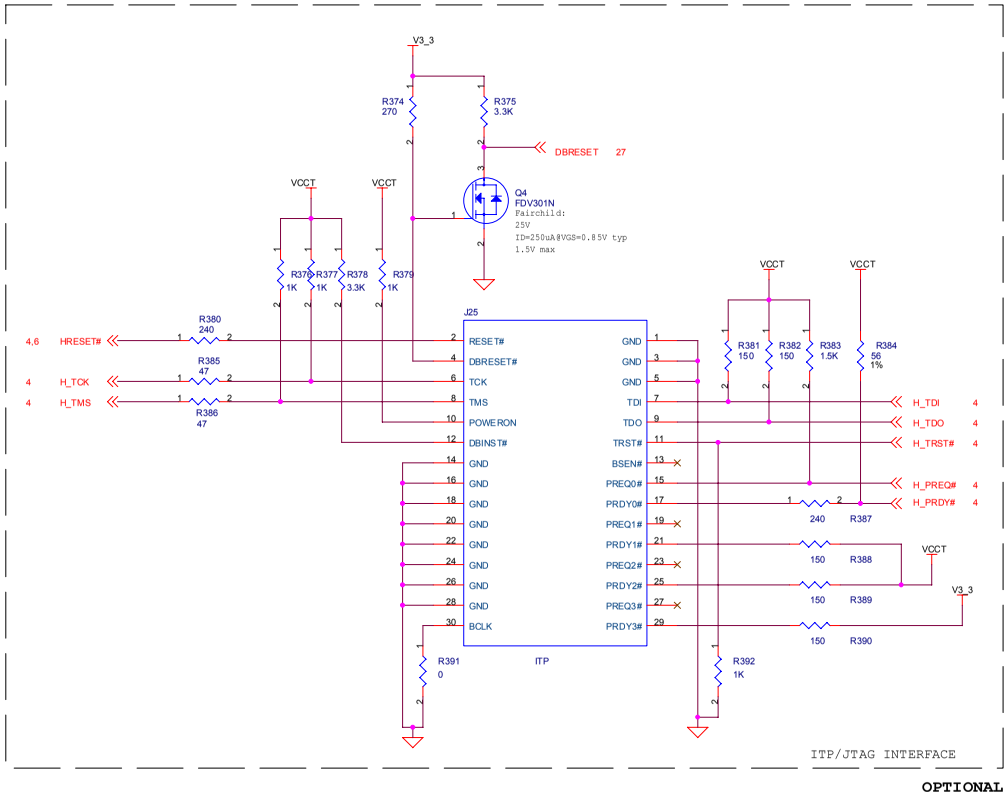
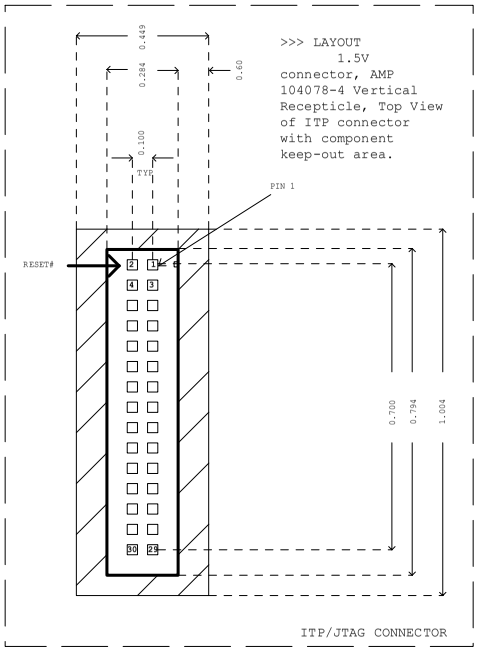
ITP, Thermal Sensor, and Clock Throttling









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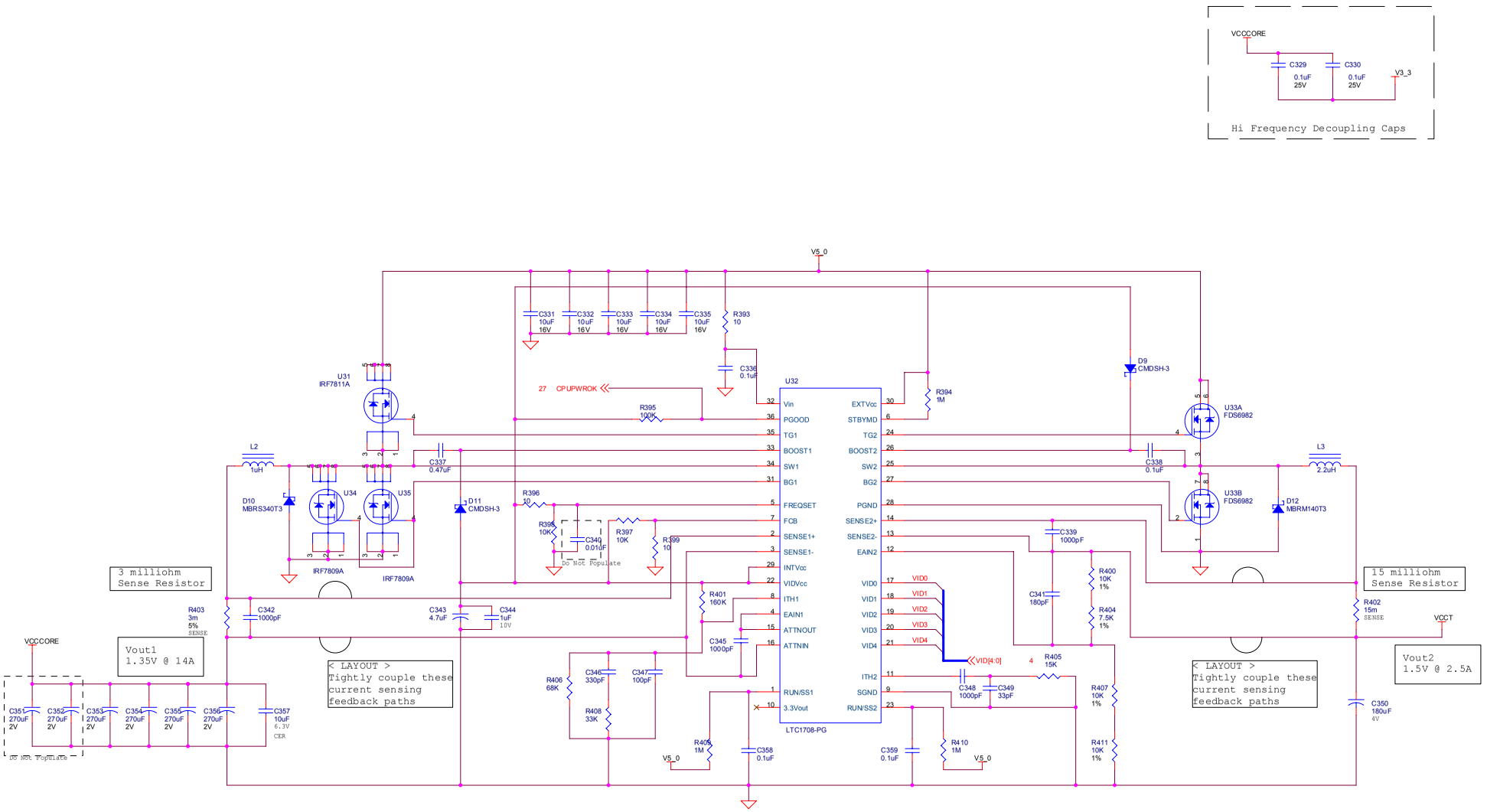
Processor Voltage Regulator



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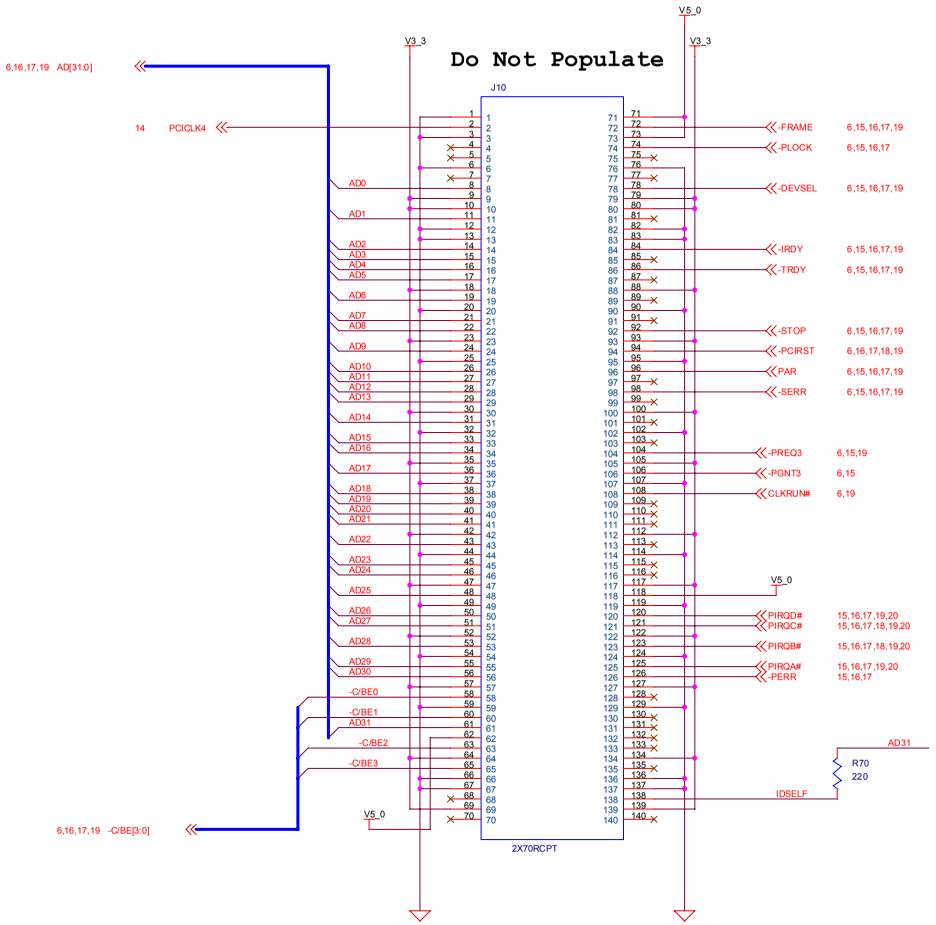
Mini PCI Connector



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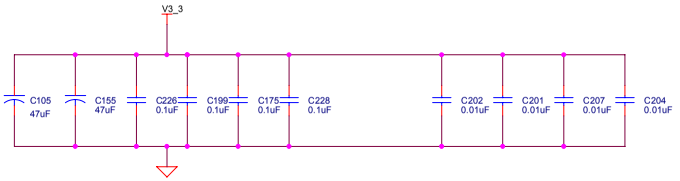
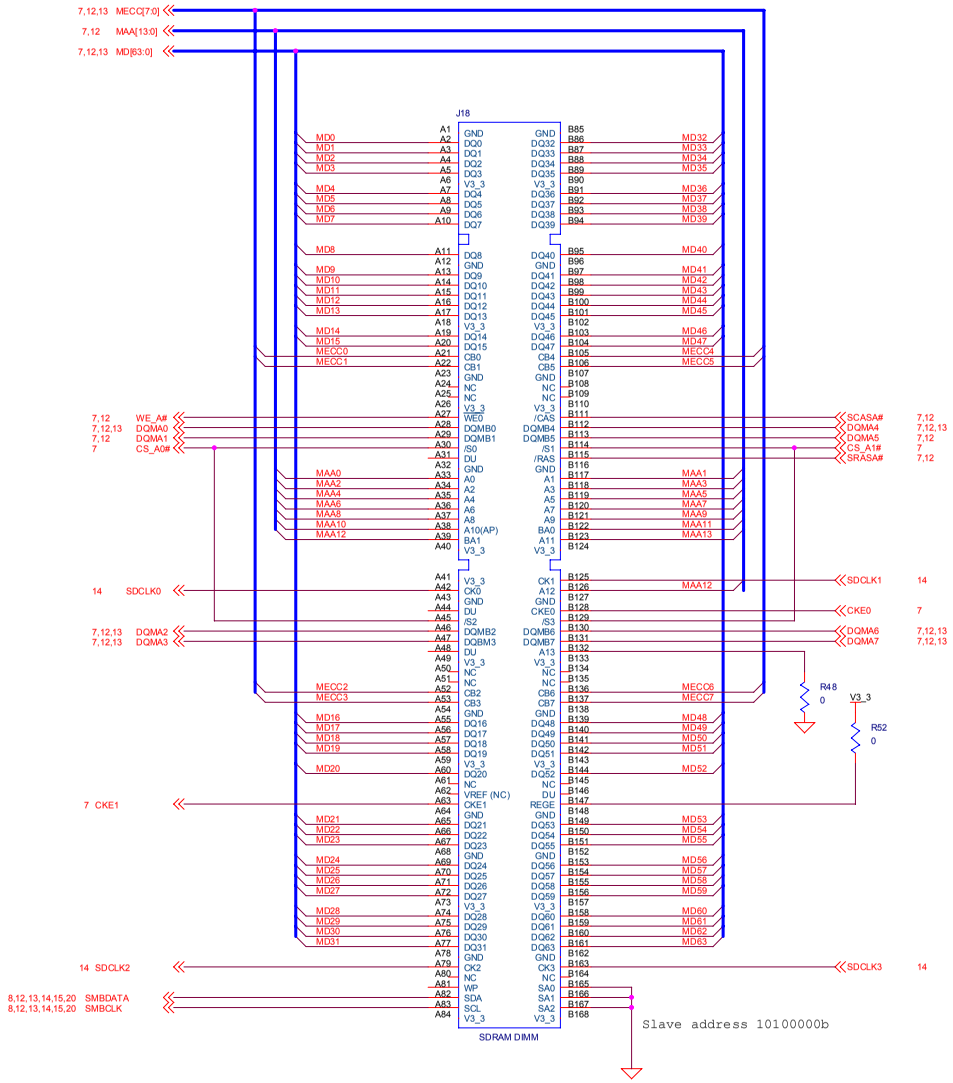
DIMM0



Socket 0



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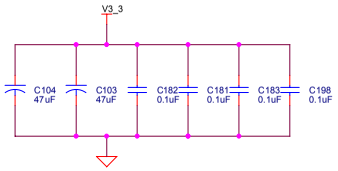
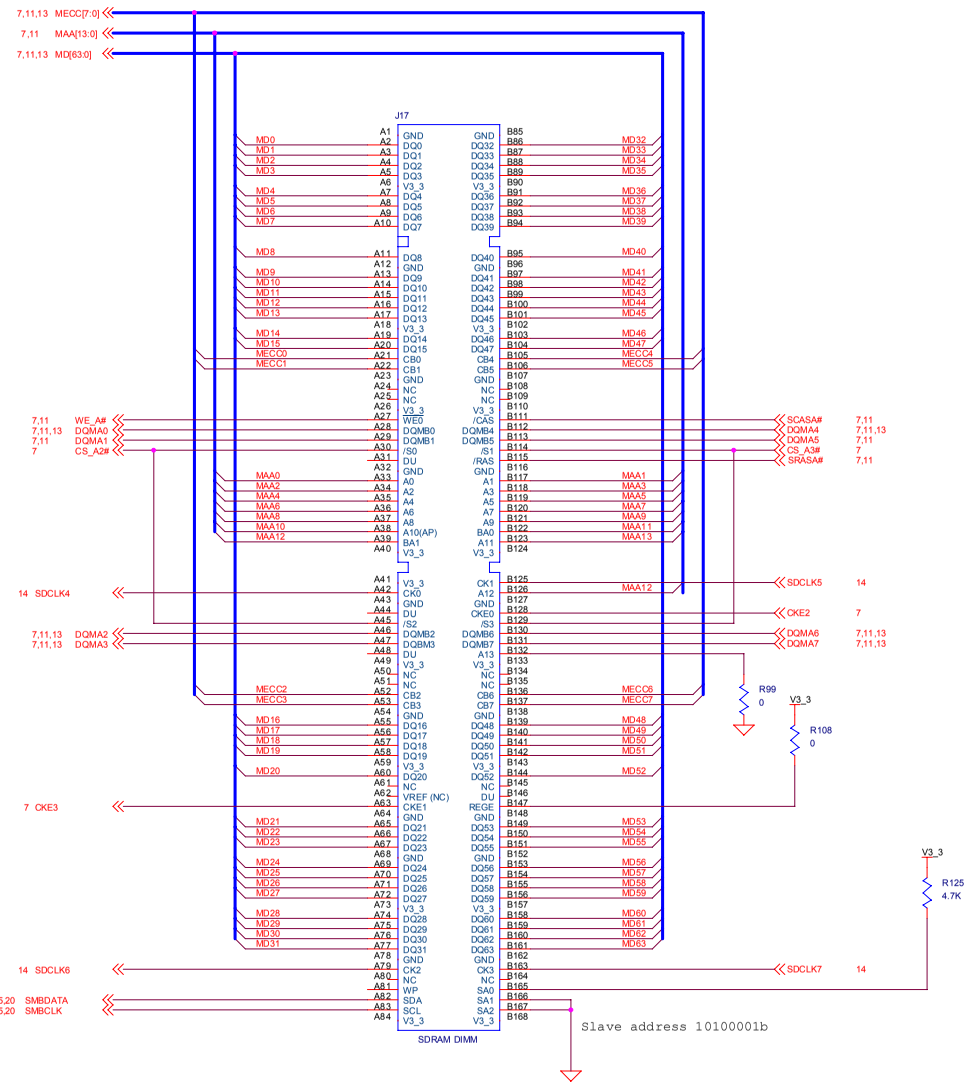
DIMM1



Socket 1



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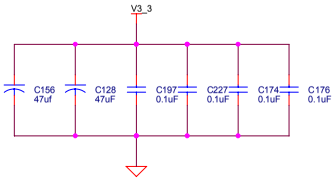
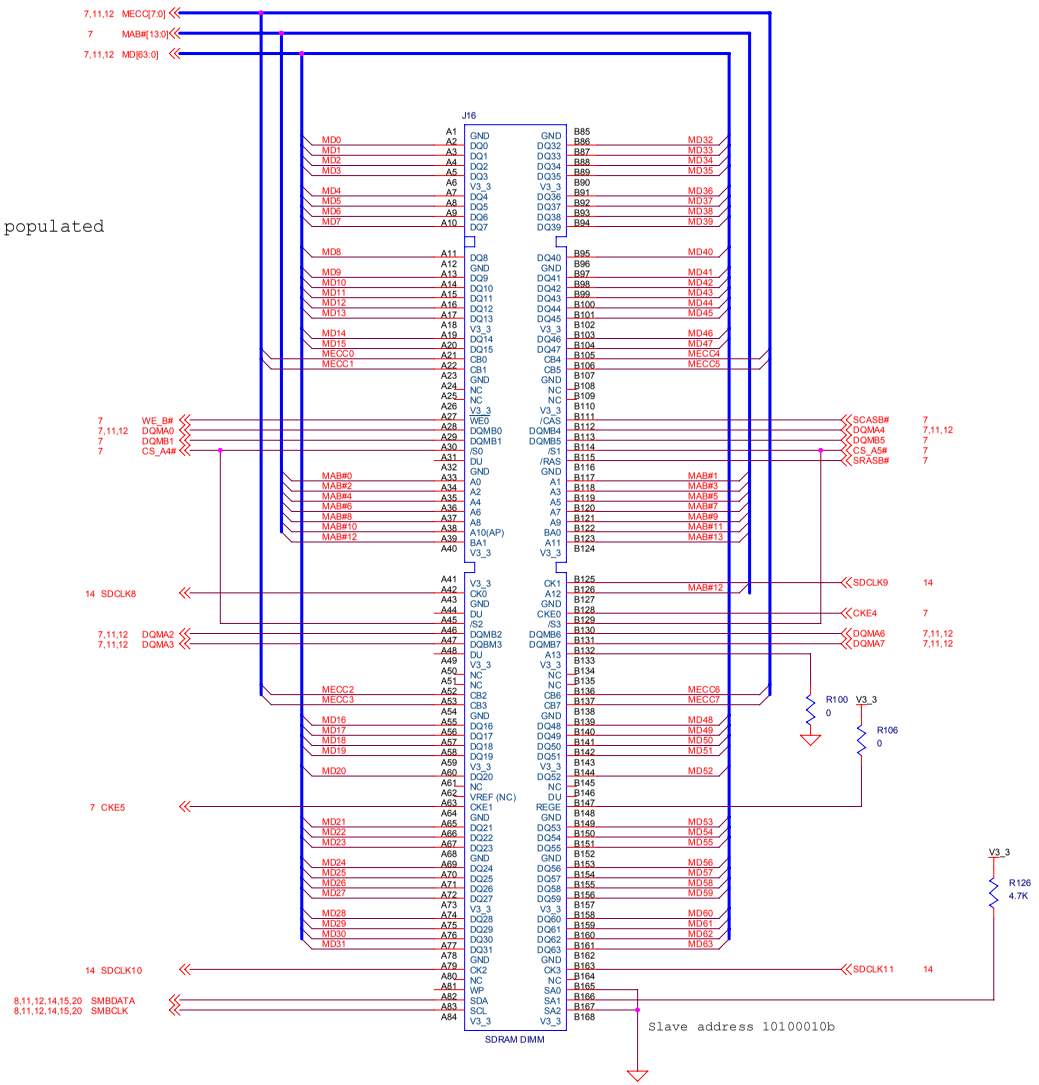
DIMM2



Socket 2

Note: J16 is not populated



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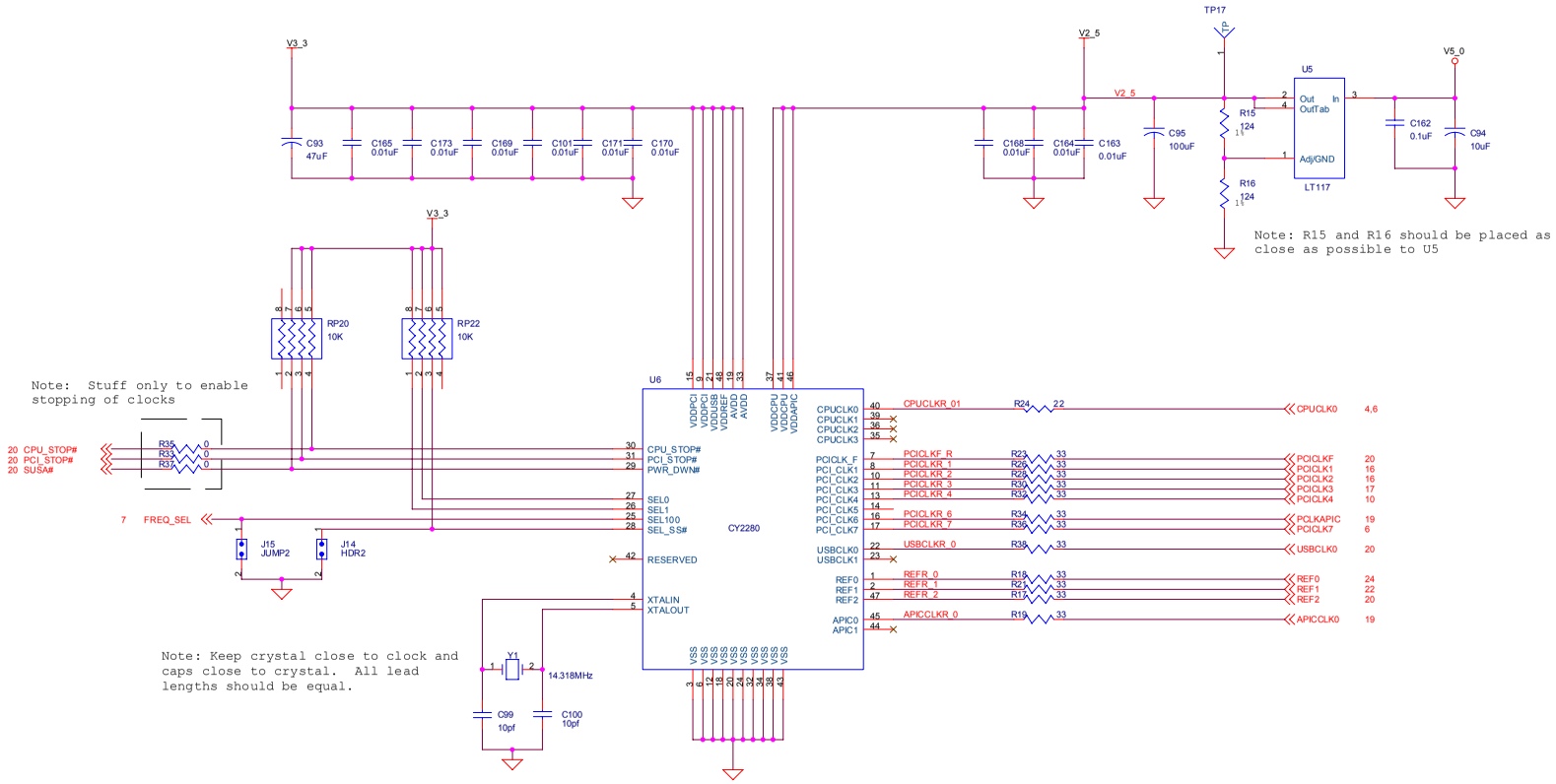
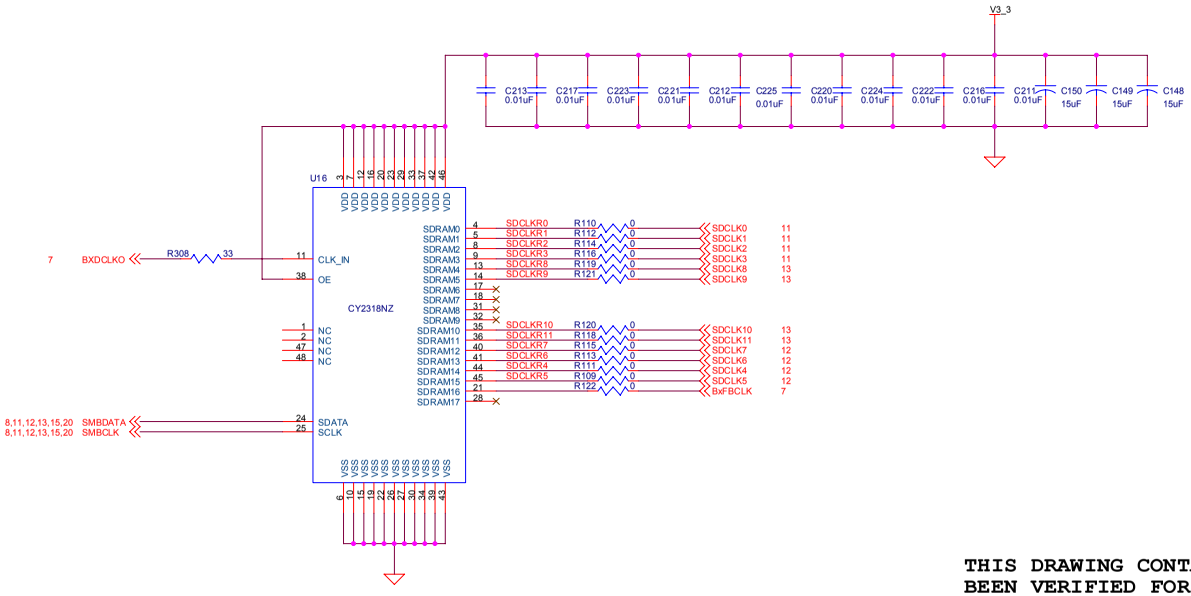
System Clocks





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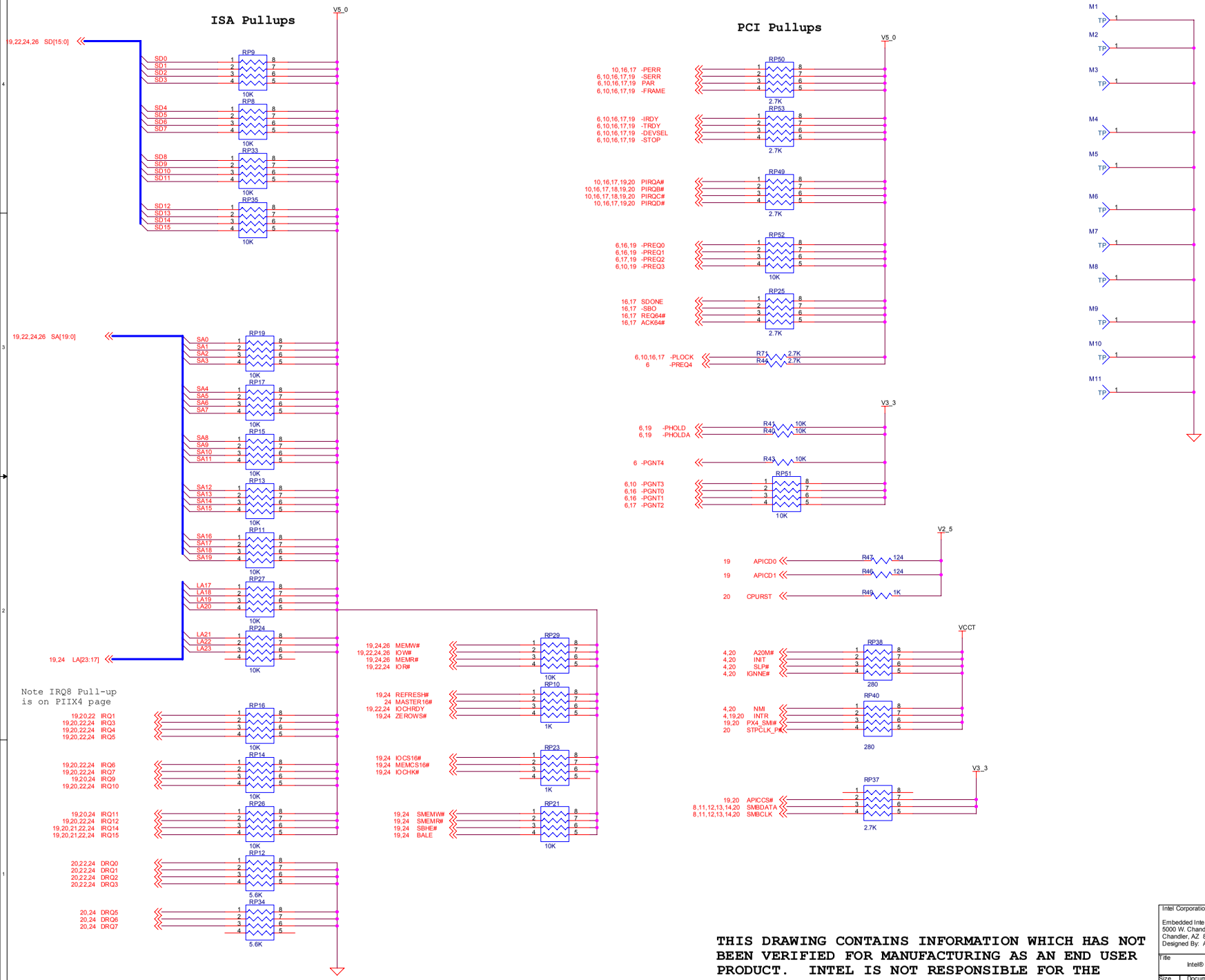
PCI / ISA Pullups



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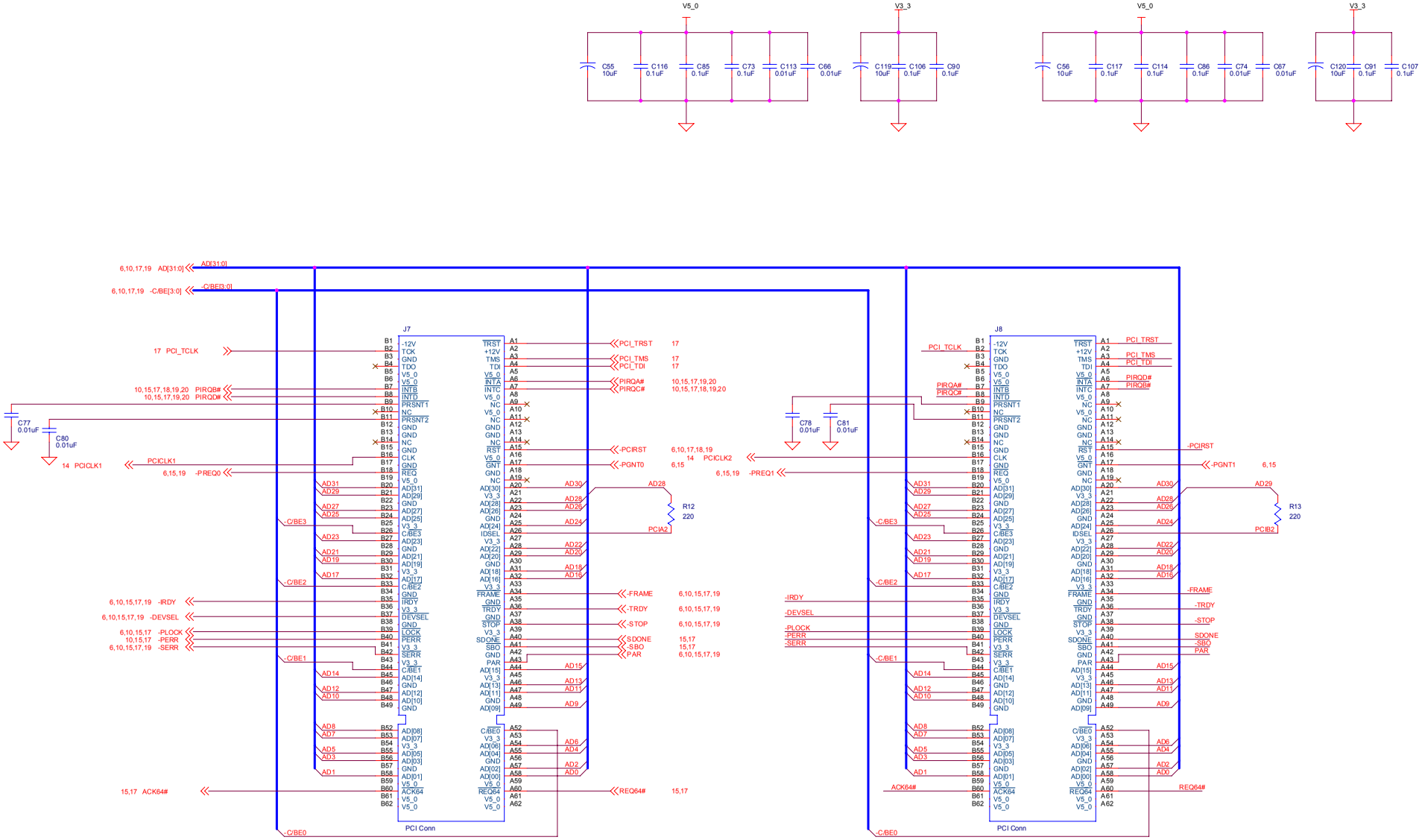
PCI Connectors 0 and 1



J7/J8 V5_0:
A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
B5, B6, B19, B22, B59, B61, B62

J7/J8 V3_3:
A21, A27, A33, A39 A45, A53
B25, B31, B36, B41, B43, B54

J7/J8 NC:
A9, A11, A14, A19
B10, B14

J7/J8 GND:
A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
B3, B12, B13, B15, B17, B28, B34, B38, B46, B49, B57

J7/J8 +12V: A2
-12V: B1

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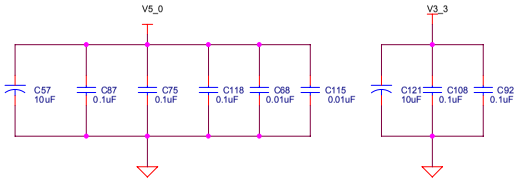
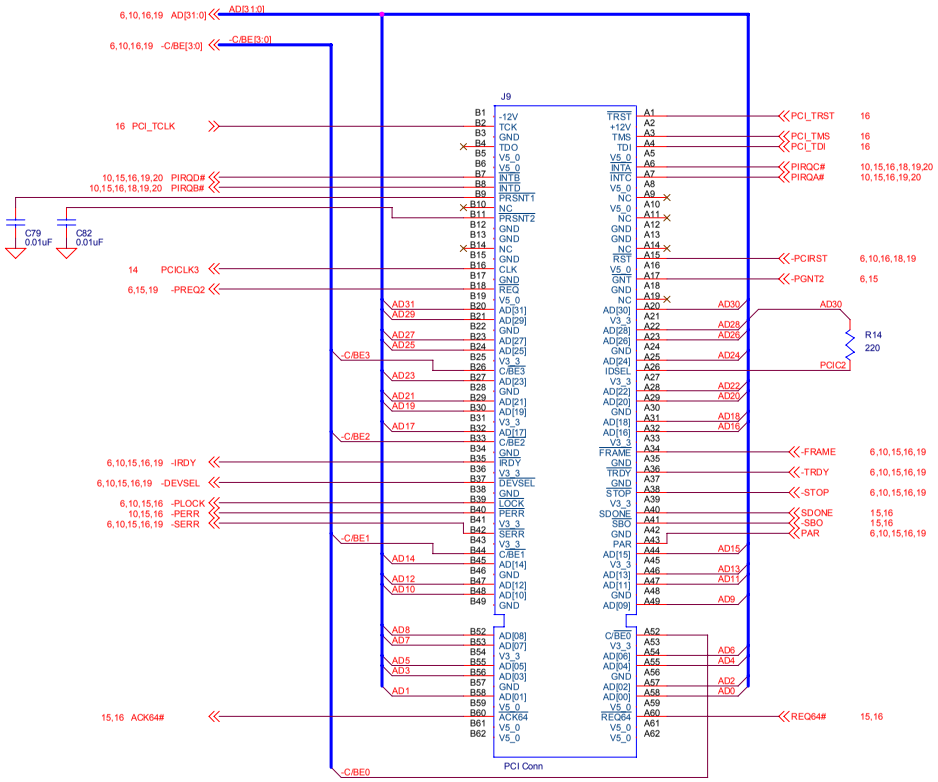
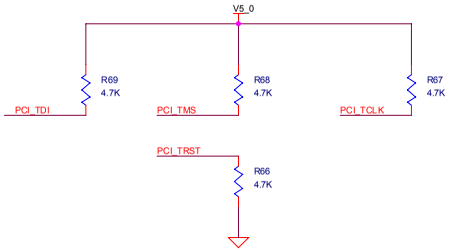
PCI Connector 2







PCI SLOT 2

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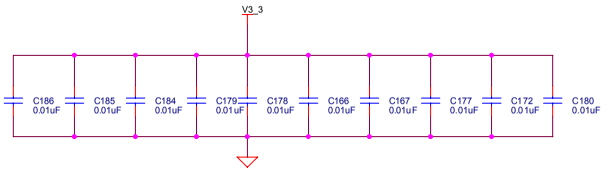
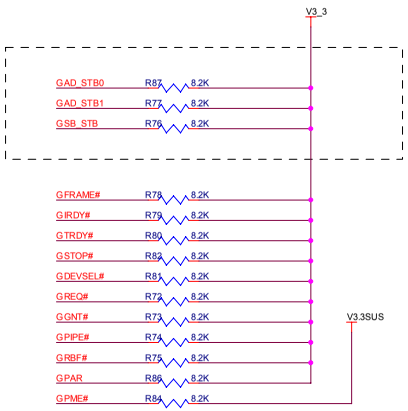
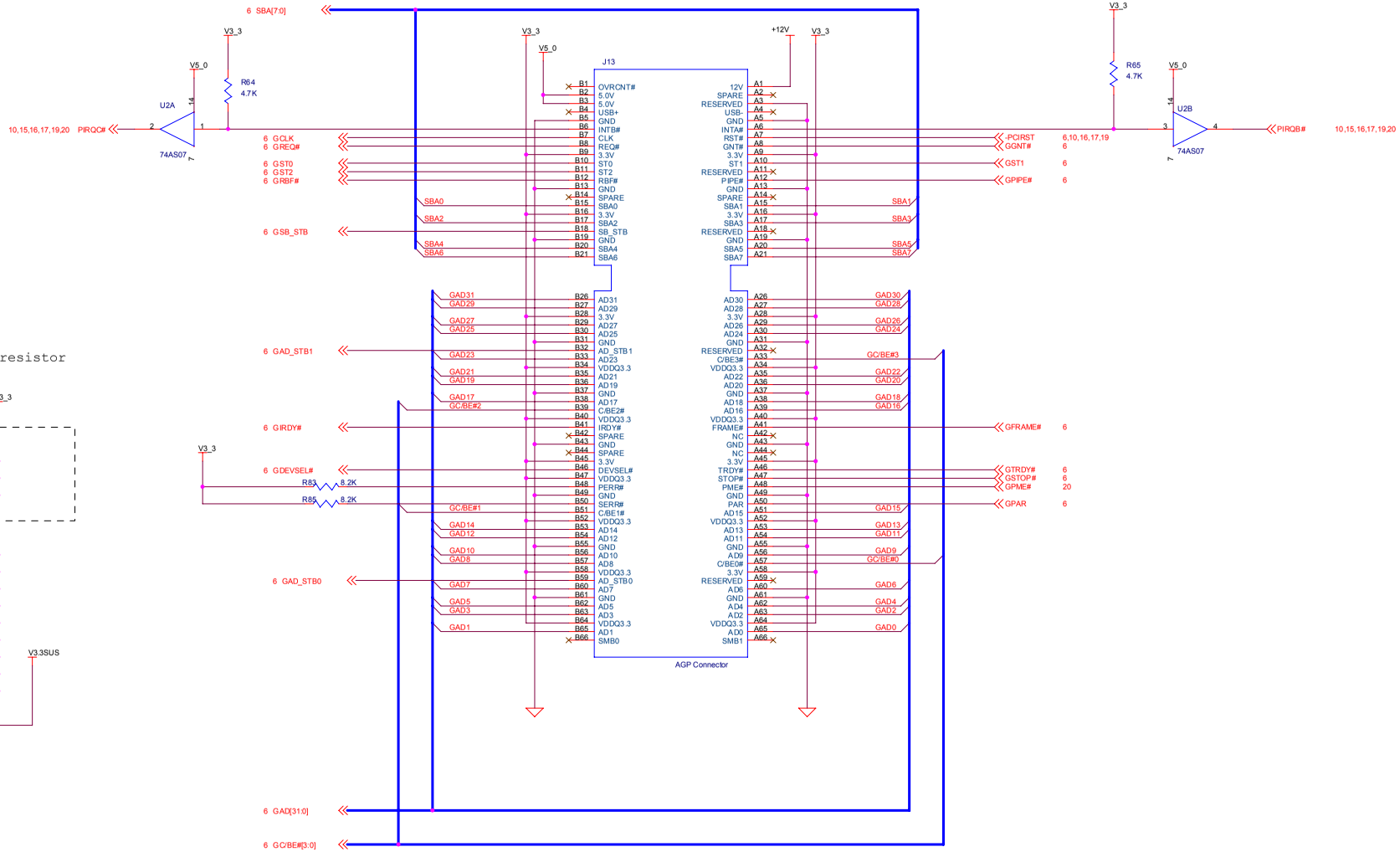
AGP Connector



Pin A3 is tied to ground per AGP Specification Rev 1.0

Stub length from connector to resistor must be less than 0.1"





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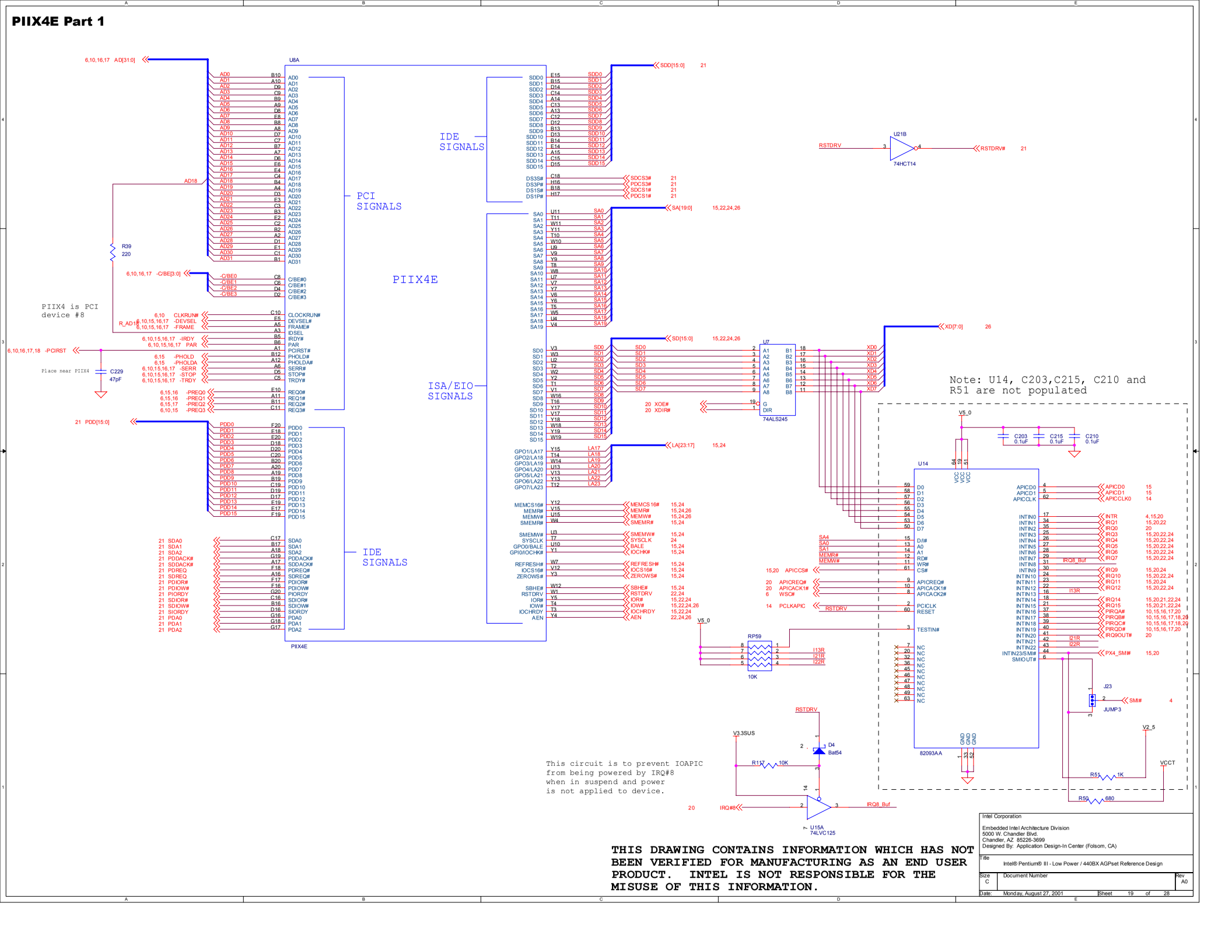
PIIX4E Part 1



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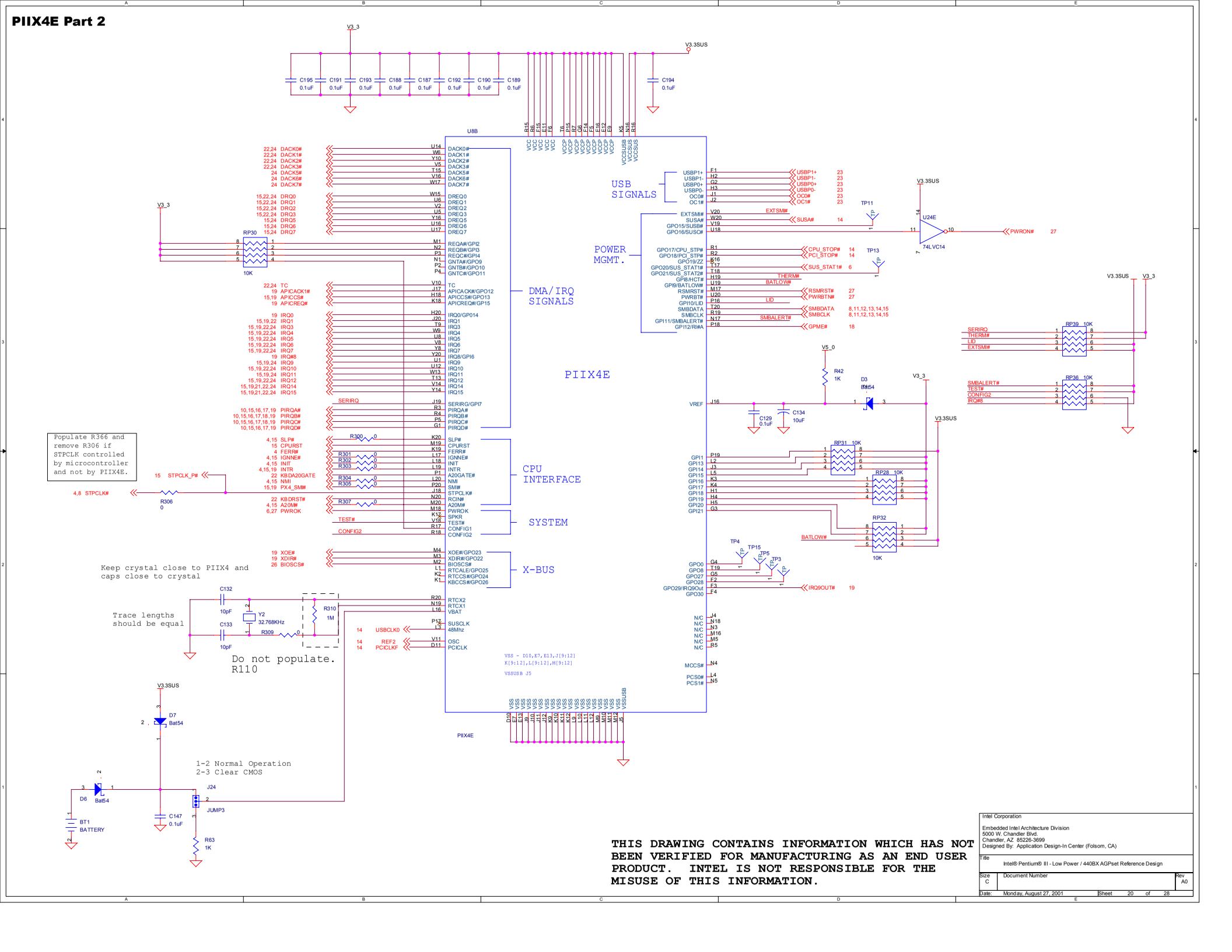
PIIX4E Part 2



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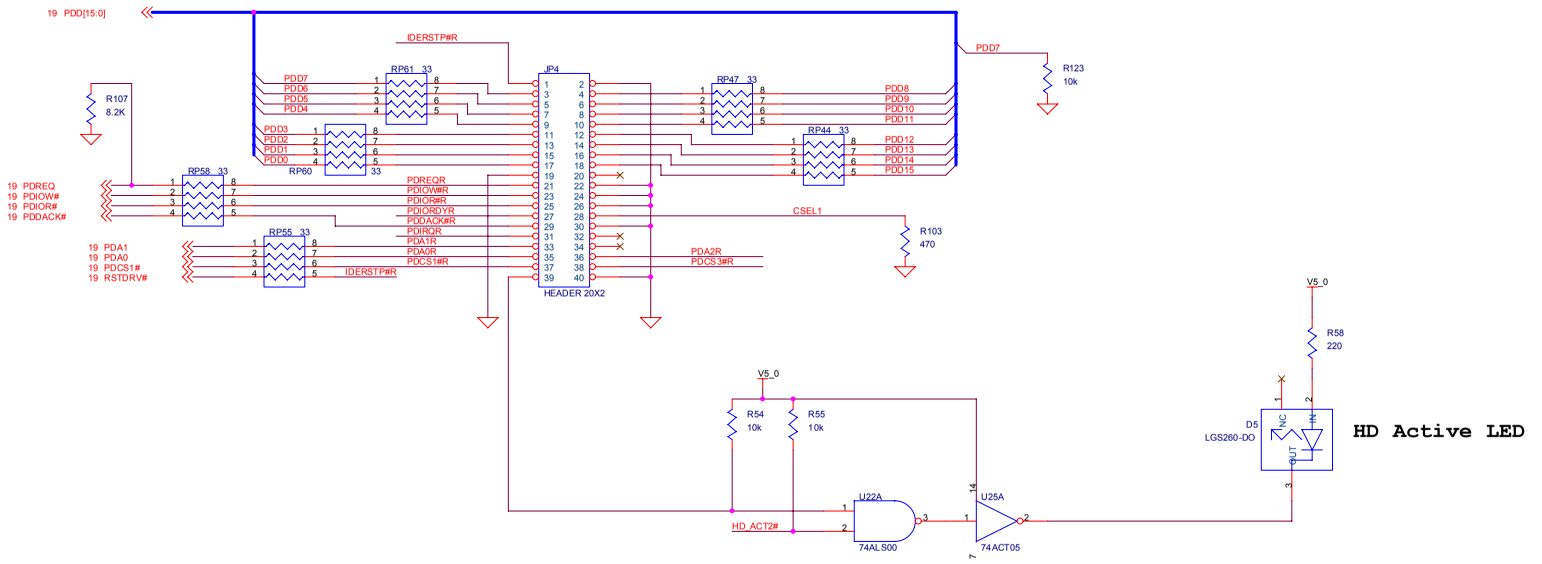
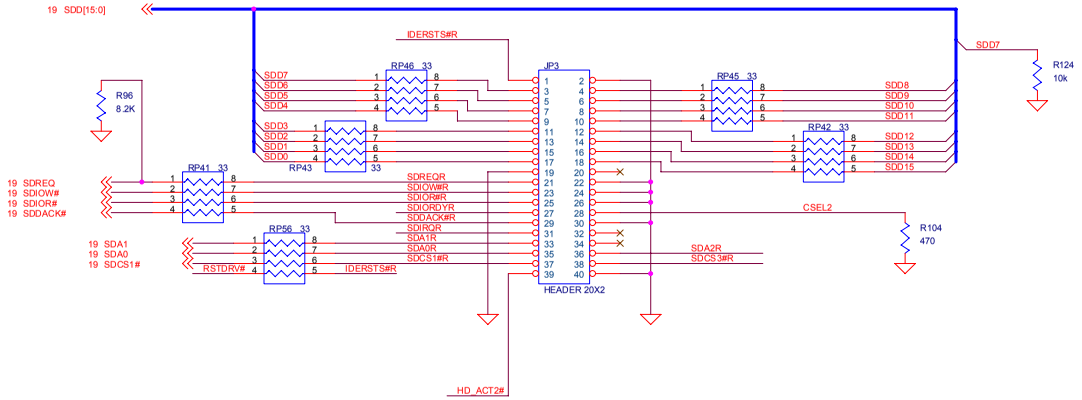
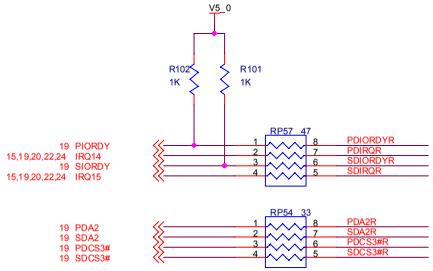
IDE Connectors

Primary IDE Connector



Secondary IDE Connector





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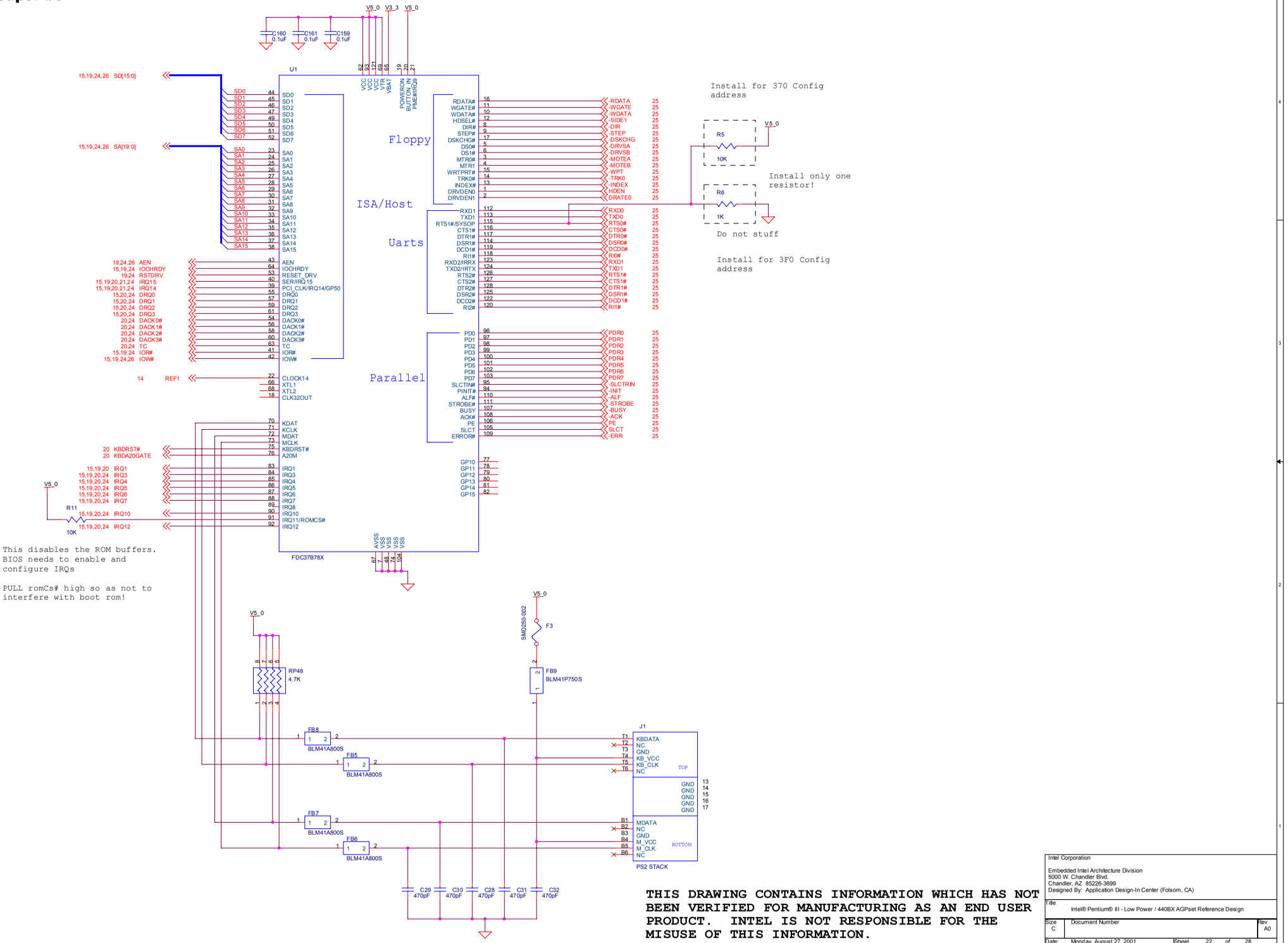
Super I/O



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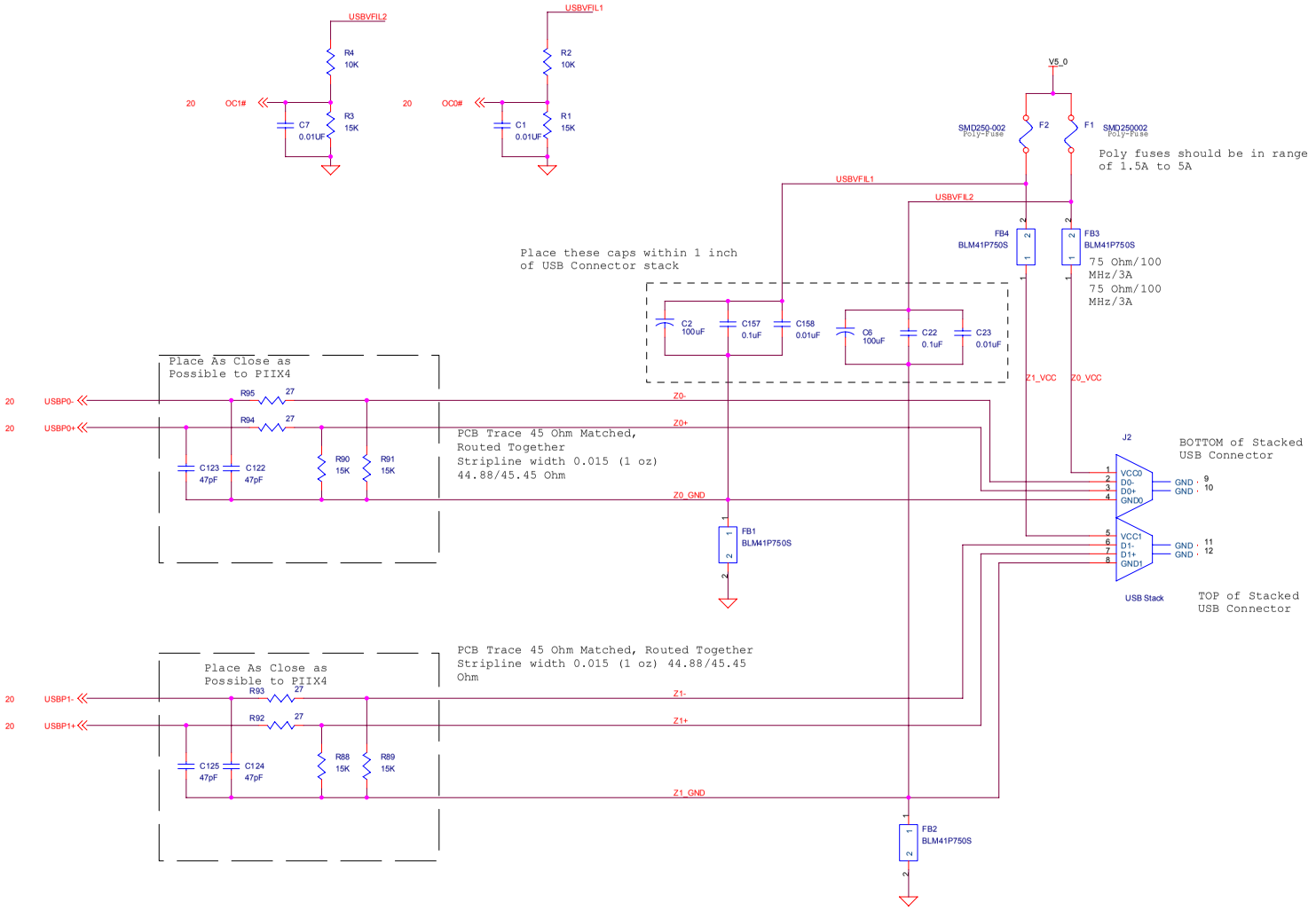
USB Connectors



NOTE 1: USB differential traces route together (Z0- & Z0+) and (Z1- & Z1+).
Must be 45 Ohm Matched
Stripline width 0.015 (for 1 oz)->44.88/45.45 Ohm.

NOTE 2: Protect differential traces w/ guard traces or
double space to any other signal.

NOTE 3: Place ferrites at connector.

NOTE 4: Poly-fuse min 1.5A
max 5A.

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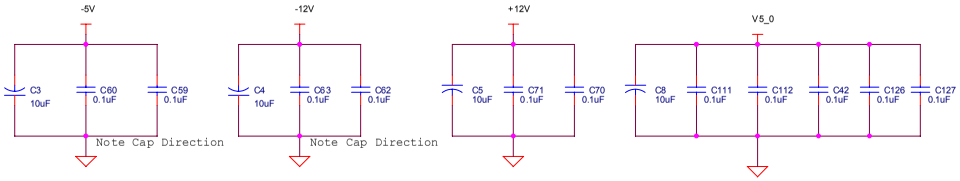
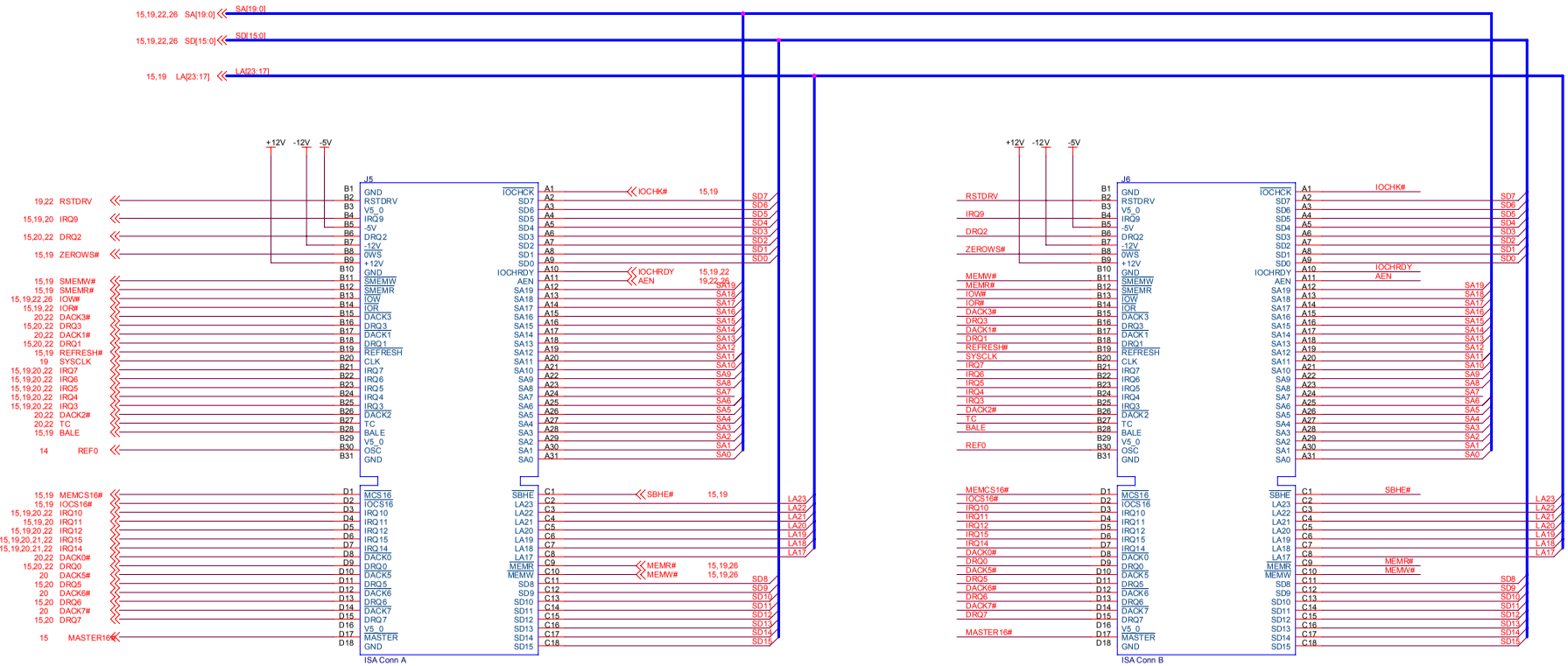
ISA Connectors





J5/J6 V5_0:
B03, B29,
B31, D16

J5/J6 GND:
B01,
B10, D18

J5/J6: +12V B09
-12V B07
-5V B05

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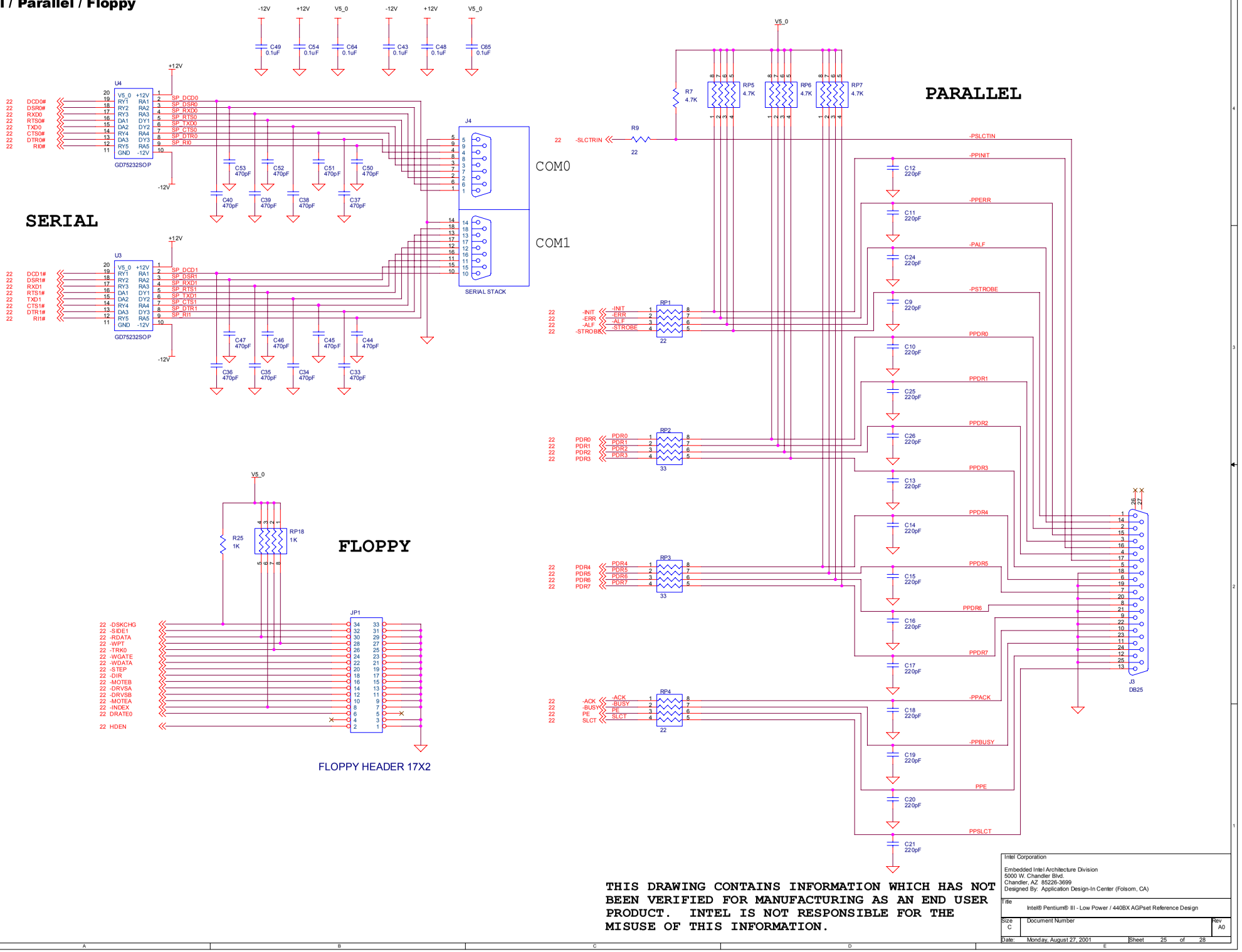
Serial / Parallel / Floppy



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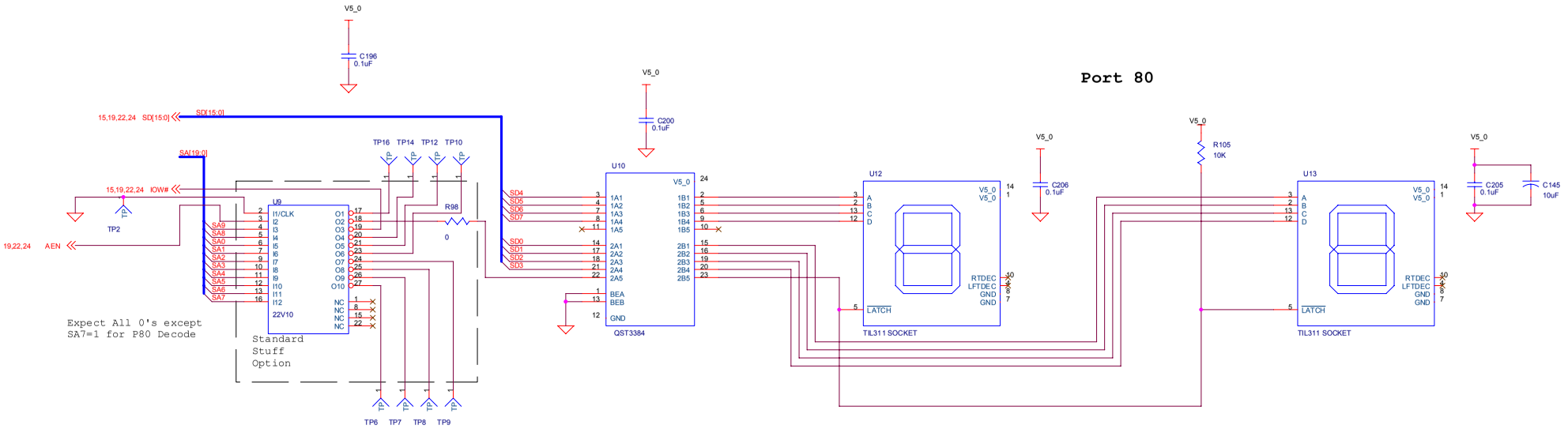
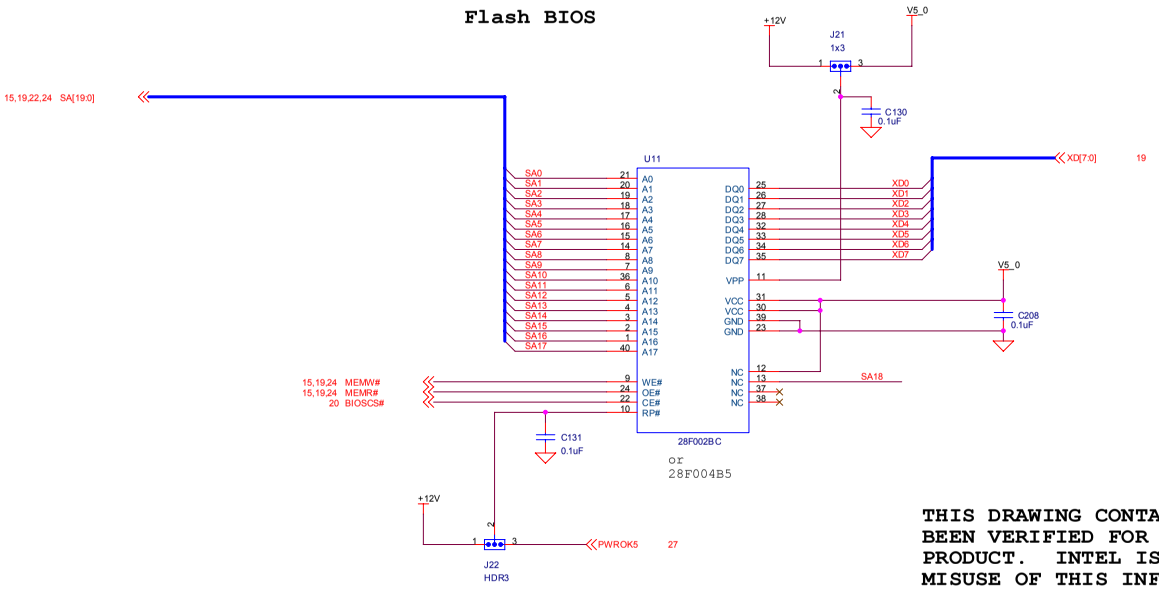
Flash BIOS / Port 80



Flash BIOS



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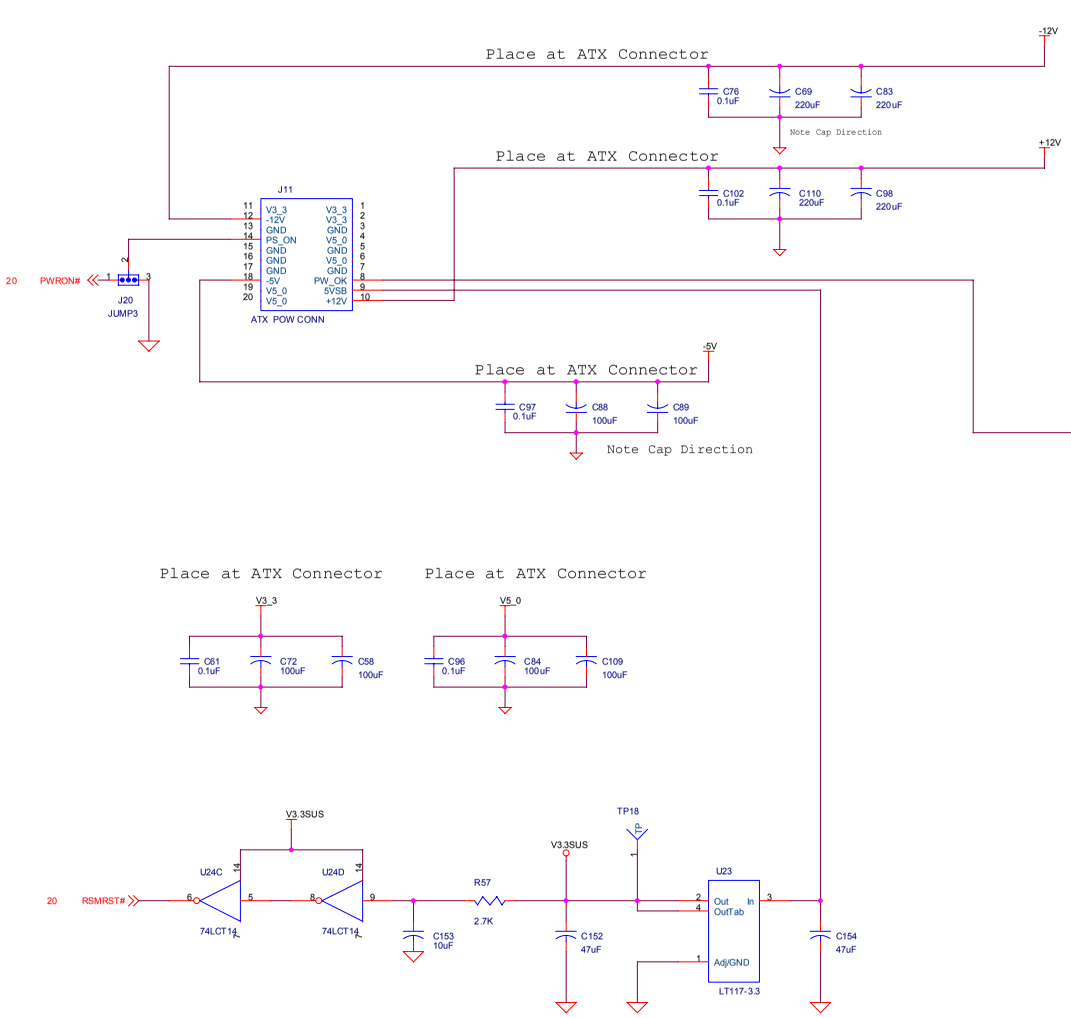
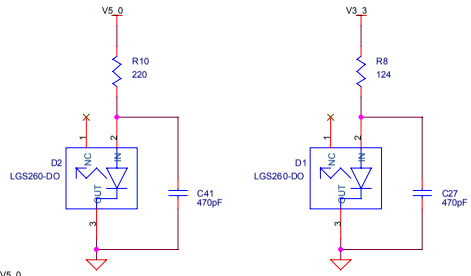
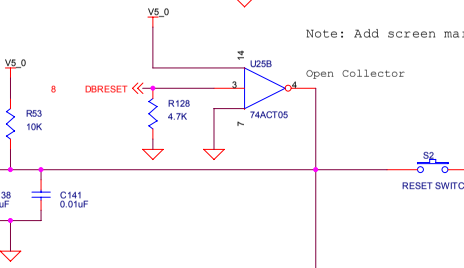
ATX Power Connector

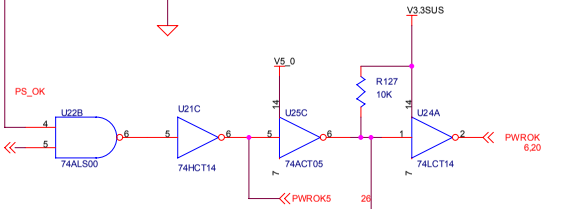


Power Indicators

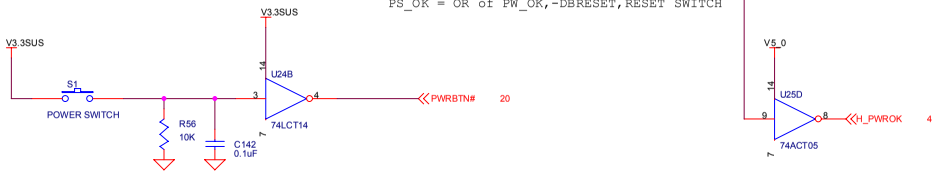


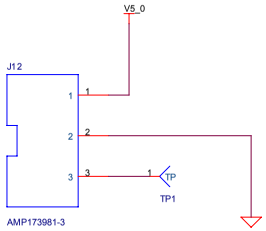
Note: Add screen marking for V5_0 LED, V3_3 LED





PS_OK = OR of PW_OK,-DBRESET,RESET SWITCH





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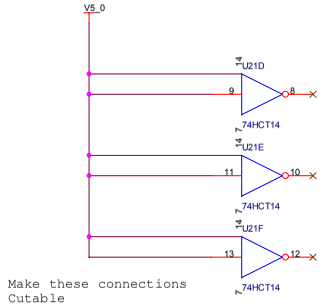
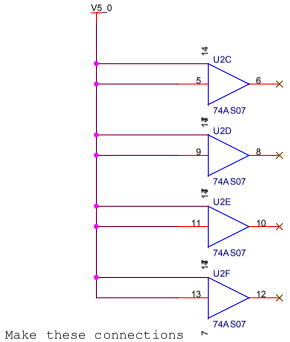
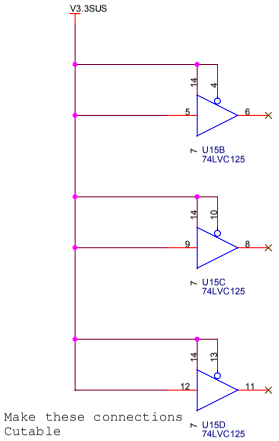
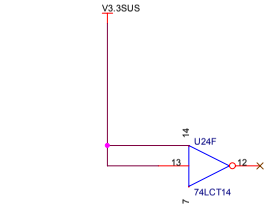
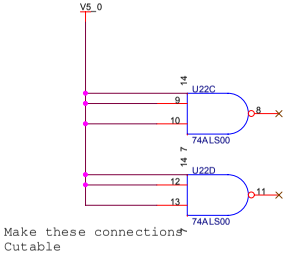
Unused Devices

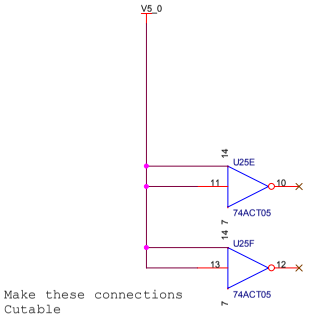












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Appendix C PLD Code Listing

The code listing below is for the 22V10 PLD.

```
TITLE       22V10 PORT 80 ADDRESS DECODER / FLASH DECODE
PATTERN     1
REVISION    B
AUTHOR      CHRIS BANYAI
COMPANY     INTEL CORPORATION
DATE        10/1/97

OPTIONS
    SECURITY = OFF


;  ( part was 22V10FN before conversion )
CHIP  P80B iPLD22V10N

PIN         19    IOWR_BAR
PIN          3    AEN
PIN      [6:7]    SA[0:1]
PIN     [9:13]    SA[2:6]
PIN         16    SA7
PIN      [5:4]    SA[8:9]
PIN    [26:23]    SA[19:16]
PIN    [21:20]    SA[15:14]
PIN          2    SEL

PIN         18   /CS_BAR
PIN         17   /CS_DOC
PIN         27    OX

EQUATIONS
CS_BAR = /IOWR_BAR * /AEN * /SA0 * /SA1 * /SA2 * /SA3 * /SA4 * /SA5 * /SA6
              * SA7 * /SA8 * /SA9
CS_BAR.TRST = VCC

CS_DOC = /SEL * /AEN * SA19 * SA18 * /SA17 * /SA16 * SA15 * /SA14
       + SEL * /AEN * SA19 * SA18 * /SA17 * SA16 * /SA15 * /SA14
CS_DOC.TRST = VCC

OX = /IOWR_BAR
OX.TRST = VCC

SIMULATION

    SETF /AEN /SA0 /SA1 /SA2 /SA3 /SA4 /SA5 /SA6 /SA7 /SA8 /SA9 IOWR_BAR
    SETF SA7 IOWR_BAR
    SETF /IOWR_BAR
    SETF IOWR_BAR
    SETF AEN /IOWR_BAR
    SETF /AEN
```

```
SETF IOWR_BAR
SETF SA0 /IOWR_BAR
SETF /SA0 /IOWR_BAR
SETF IOWR_BAR
SETF /SA0 /SA1 /SA2 /SA3 /SA4 /SA5 /SA6 /SA7 /SA8 /SA9
SETF /SA19 /SA18 /SA17 /SA16 /SA15 /SA14
SETF /SEL
SETF SA19 SA18 /SA17 /SA16 SA15 /SA14
SETF /SEL
SETF /AEN
SETF /SA19
SETF SA19
SETF /SA18
SETF SA18
SETF SA17
SETF /SA17
SETF SA16
SETF /SA16
SETF /SA15
SETF SA15
SETF SA14
SETF /SA14
SETF /SEL
SETF SA19 SA18 /SA17 SA16 /SA15 /SA14
SETF /SEL
SETF /AEN
SETF SEL
SETF /SA19
SETF SA19
SETF /SA18
SETF SA18
SETF SA17
SETF /SA17
SETF /SA16
SETF SA16
SETF SA15
SETF /SA15
SETF SA14
SETF /SA14
SETF /SEL
```